

LLW-1/LGG-1 Schematics

Sandy Bridge

Cougar Point

2011-01-18

REV : -1

DY:None Installed

UMA:UMA platform installed only

PX:Discrete(both Robson and Whistler) SKU installed

RBS:Robson SKU installed only

WTL:Whistler SKU installed only

SAMSUNG:Use SAMSUNG VRAM

Hynix:Use Hynix VRAM

VRAM_1G:Use 1G VRAM

VRAM_2G:Use 2G VRAM

<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover Page

Size
A3

Document Number

LLW-1 / LGG-1

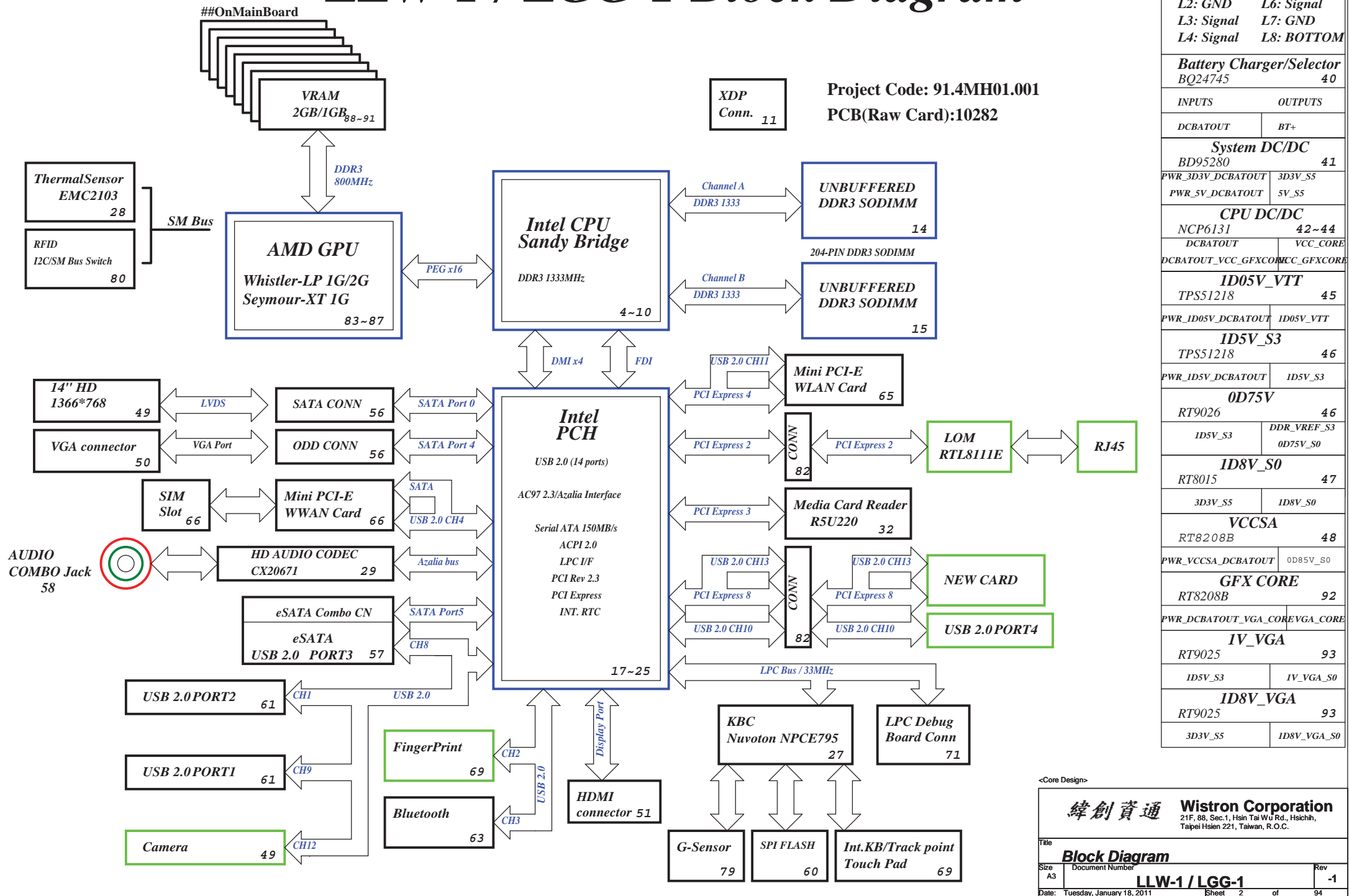
Rev

-1

Date: Tuesday, January 18, 2011

Sheet 1 of 94

LLW-1 / LGG-1 Block Diagram



1

2

3

4

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	Enable Danbury: Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. Disable Danbury: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] Disable Danbury: Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

USB Table

PCIE Routing

LANE1	RESERVED
LANE2	LAN
LANE3	CARD READER
LANE4	MiniCard WLAN
LANE5	RESERVED
LANE6	RESERVED
LANE7	RESERVED
LANE8	NEW CARD

SATA Table

SATA	
Pair	Device
0	HDD
1	mSATA
2	N/A
3	N/A
4	ODD
5	ESATA

Pair	Device
0	X
1	USB2
2	FINGERPRINT
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	X
6	X
7	X
8	ESATA1
9	USB1
10	USB Ext. port 4
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

C

E

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	PCI-Express Port Bifurcation Straps	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	PEG DEFER TRAINING	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training	

POWER PLANE	VOLTAGE	Voltage Rails	
		ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

SMBus ADDRESSES

I ² C / SMBus Addresses		HURON RIVER ORB		
Device	Ref Des	Address	Hex	Bus
EC SMBus 1 Battery Capacity Board				KBC_SDA1/KBC_SCL1 KBC_SDA1/KBC_SCL1
EC SMBus 2 PCH MXM LCD Thermal Sensor				KBC_SDA2/KBC_SCL2 KBC_SDA2/KBC_SCL2 KBC_SDA2/KBC_SCL2 KBC_SDA2/KBC_SCL2 KBC_SDA2/KBC_SCL2
PCH SMBus CKS05 Clock Generator SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Table of Content			
Size	Document Number		Rev
A3	LLW-1 / LGG-1		-1
Date:	Tuesday, Januaru 18, 2011	Sheet	3 of 94

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

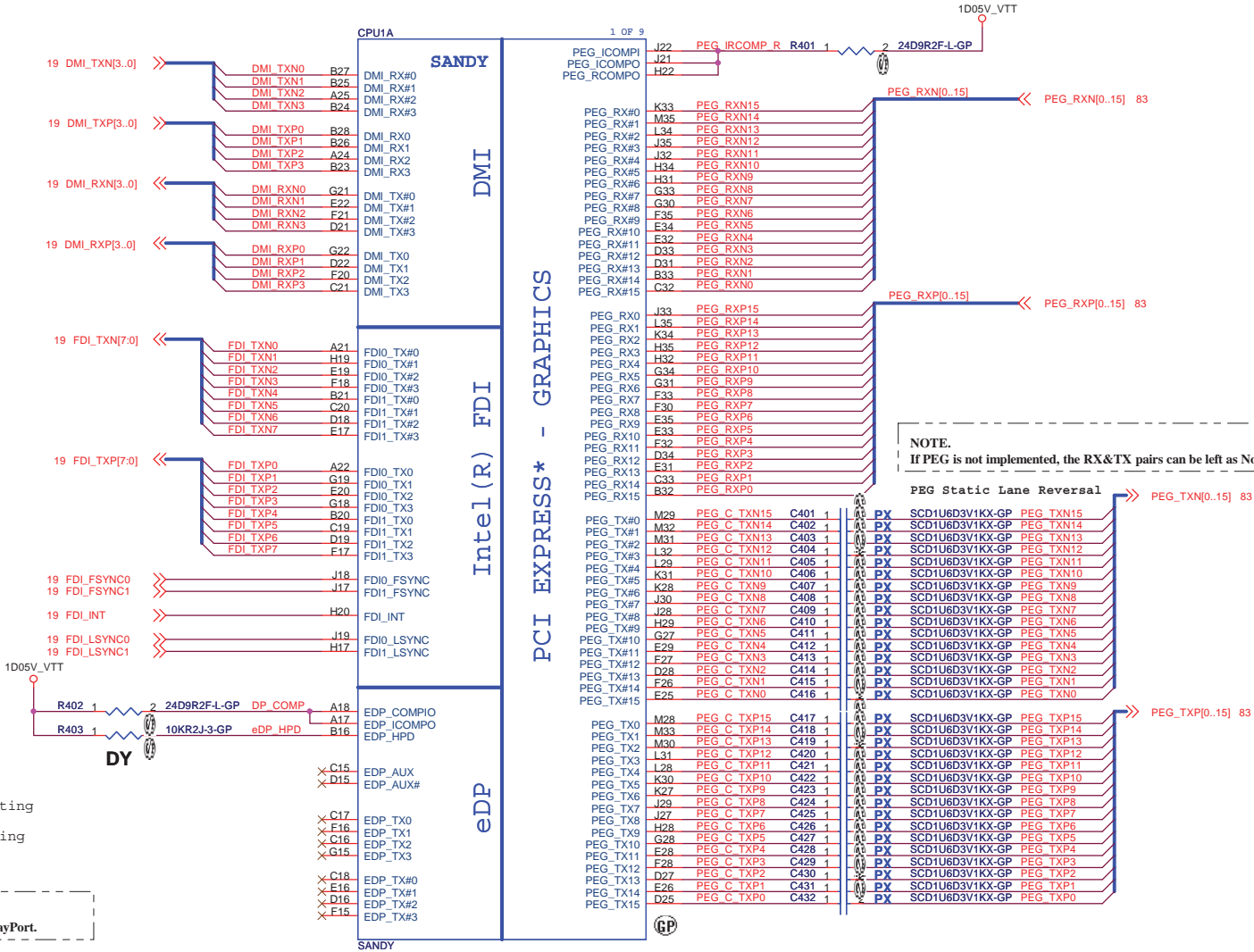


Table 4.1- Central Processing Unit slot multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
FOXCONN	PZ98827-364B-41F	N/A	62.10055.421
TYCO	2-2013620-3	N/A	62.10040.771

<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU (PCIE/DMI/FDI)

Size

Document Number

Rev

-1

Date

Tuesday, January 18, 2011

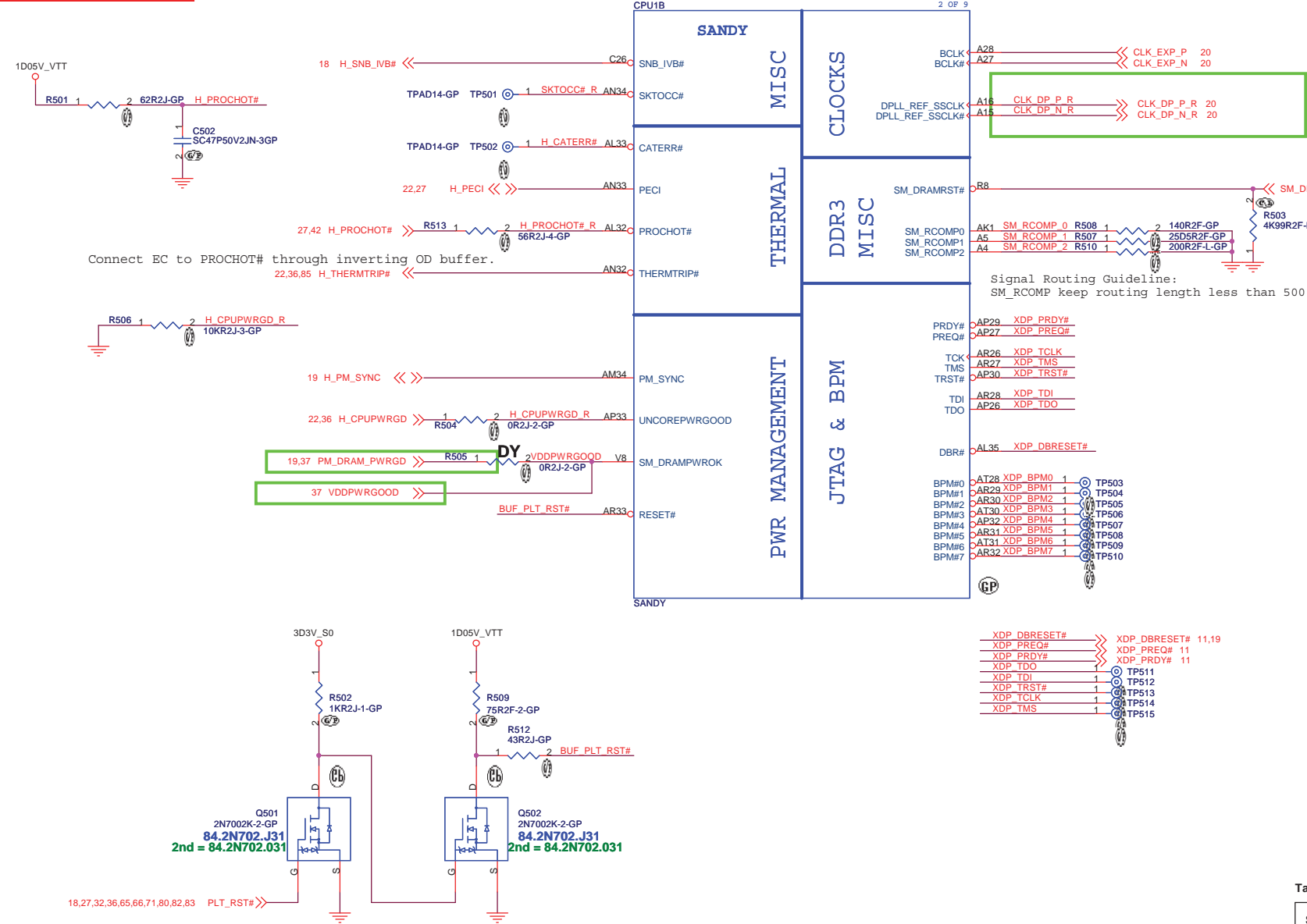
Sheet

4

of

94

SSID = CPU



Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.

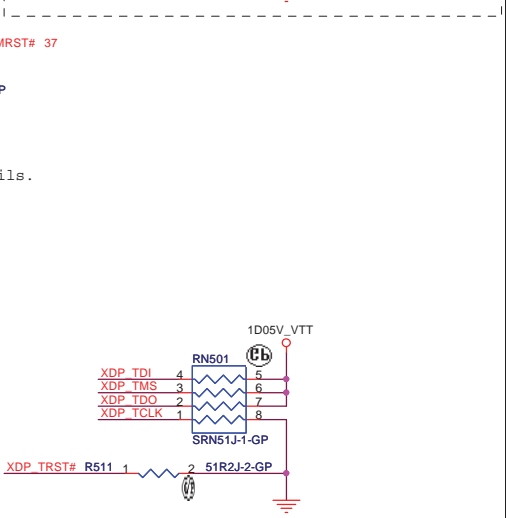


Table 5.1- N-Channel MOSFET multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
PANJIT	2N7002K	N/A	84.2N702.J31
DIODES	2N7002K	N/A	84.2N702.031
NXP	2N7002BK	N/A	84.07002.I31

<Core Design>

緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

Size A3

Date: Tuesday, January 18, 2011

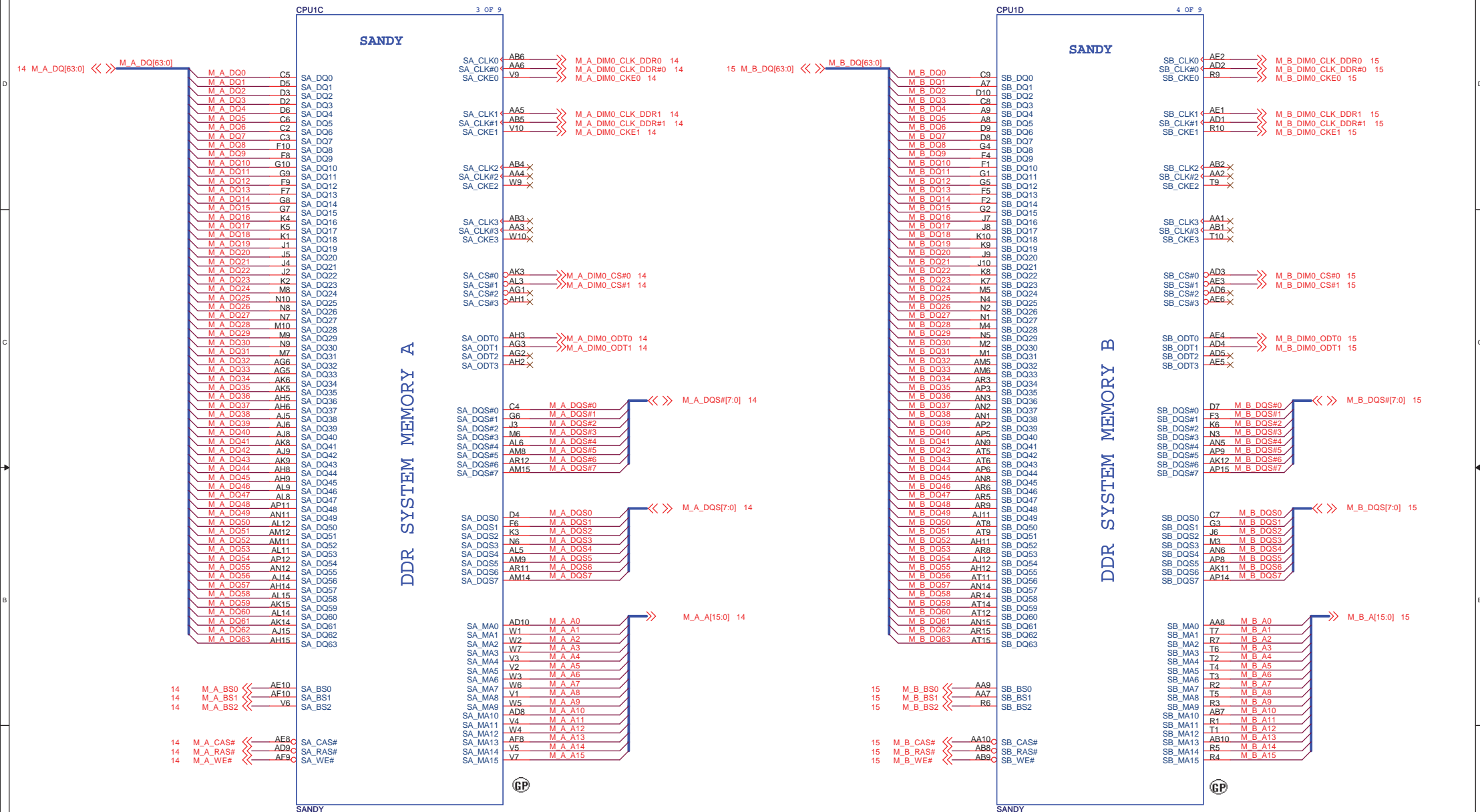
Document Number

Sheet 5 of 94

Rev -1

LLW-1 / LGG-1

SSID = CPU

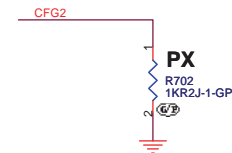
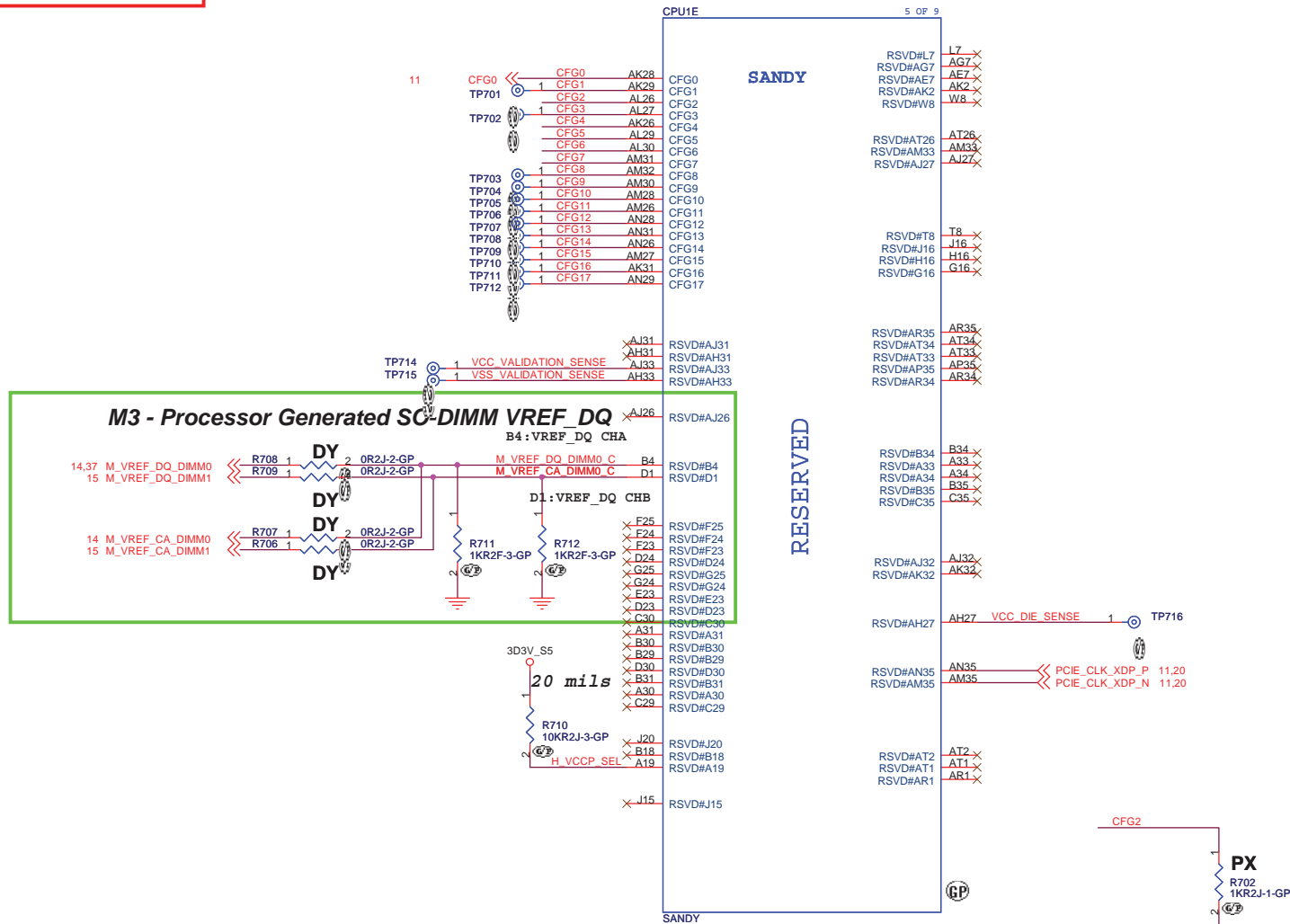


<Core Design>

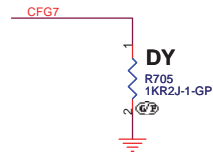
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		CPU (DDR)	
Size	A3	Document Number	LLW-1 / LGG-1
Date:	Tuesday, January 18, 2011	Sheet	6 of 94
Rev	-1		

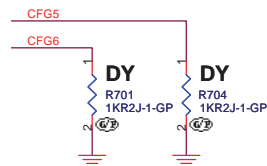
SSID = CPU



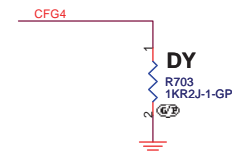
PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	0: Lane Reversed



PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

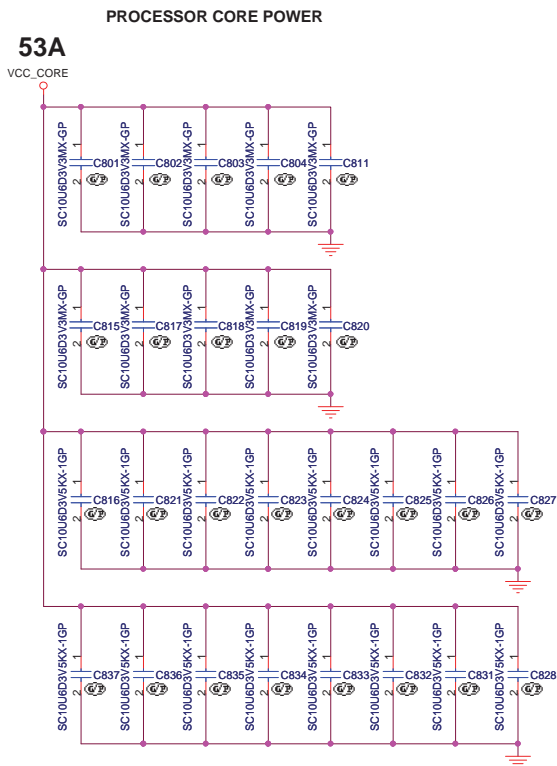


PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled; function 2 disabled 01: Reserved (Device 1 function 1 disabled; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



Display Port Presence Strap	
CFG4	<p>1: Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0: Enabled; An external Display Port device is connected to the Embedded Display Port</p>

SSID = CPU



VCC Output Decoupling Recommendation:
4 x 470 uF at Bottom Socket Edge
8 x 22 uF at Top Socket Cavity
8 x 22 uF at Top Socket Edge
8 x 22 uF at Bottom Socket Cavity

VCC_CORE

AG35 VCC
AG34 VCC
AG33 VCC
AG32 VCC
AG31 VCC
AG30 VCC
AG29 VCC
AG28 VCC
AG27 VCC
AG26 VCC
AF35 VCC
AF34 VCC
AF33 VCC
AF32 VCC
AF31 VCC
AF30 VCC
AF29 VCC
AF28 VCC
AF27 VCC
AD35 VCC
AD34 VCC
AD33 VCC
AD32 VCC
AD31 VCC
AD30 VCC
AD29 VCC
AD28 VCC
AD27 VCC
AC35 VCC
AC34 VCC
AC33 VCC
AC32 VCC
AC31 VCC
AC30 VCC
AC29 VCC
AC28 VCC
AC27 VCC
AC26 VCC
AA35 VCC
AA34 VCC
AA33 VCC
AA32 VCC
AA31 VCC
AA30 VCC
AA29 VCC
AA28 VCC
AA27 VCC
AA26 VCC
Y35 VCC
Y34 VCC
Y33 VCC
Y32 VCC
Y31 VCC
Y30 VCC
Y29 VCC
Y28 VCC
Y27 VCC
Y26 VCC
Y35 VCC
Y34 VCC
Y33 VCC
Y32 VCC
Y31 VCC
Y30 VCC
Y29 VCC
Y28 VCC
Y27 VCC
Y26 VCC
U35 VCC
U34 VCC
U33 VCC
U32 VCC
U31 VCC
U30 VCC
U29 VCC
U28 VCC
U27 VCC
U26 VCC
R35 VCC
R34 VCC
R33 VCC
R32 VCC
R31 VCC
R30 VCC
R29 VCC
R28 VCC
R27 VCC
R26 VCC
P35 VCC
P34 VCC
P33 VCC
P32 VCC
P31 VCC
P30 VCC
P29 VCC
P28 VCC
P27 VCC
P26 VCC

SANDY

POWER

SANDY

CORE SUPPLY

SVID

SENSE LINES

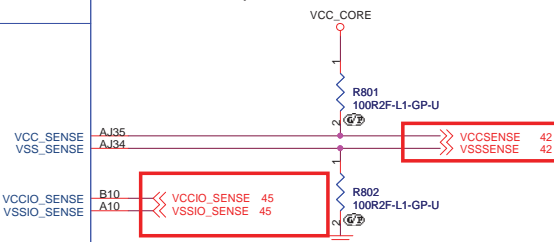
PEG AND DDR

VCCIO AH13
VCCIO AH10
VCCIO AG10
VCCIO AG10
VCCIO Y10
VCCIO L10
VCCIO P10
VCCIO J14
VCCIO J13
VCCIO J12
VCCIO J11
VCCIO H14
VCCIO H12
VCCIO H11
VCCIO G14
VCCIO G13
VCCIO G12
VCCIO F14
VCCIO F13
VCCIO F12
VCCIO F11
VCCIO E14
VCCIO E12
VCCIO E11
VCCIO D14
VCCIO D13
VCCIO D12
VCCIO D11
VCCIO C14
VCCIO C13
VCCIO C12
VCCIO C11
VCCIO B14
VCCIO B12
VCCIO A14
VCCIO A13
VCCIO A12
VCCIO A11
VCCIO J23

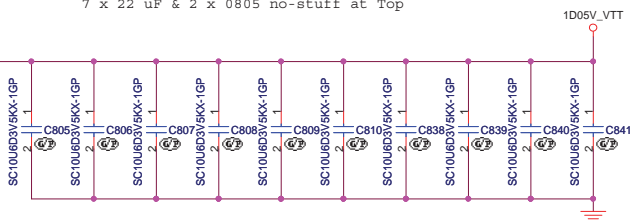
VIDALERT#
VIDCLK#
VIDSOUT

AJ29 H_CPU_SVIDALRT# R803 1 2 43R2J-GP VR_SVID_ALERT# 42
AJ30 H_CPU_SVIDCLK H_CPU_SVIDCLK 42
AJ28 H_CPU_SVIDDAT H_CPU_SVIDDAT 42

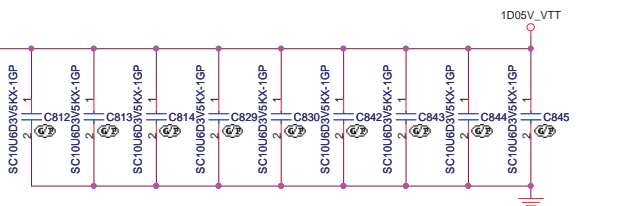
R801, R802 need to close to CPU



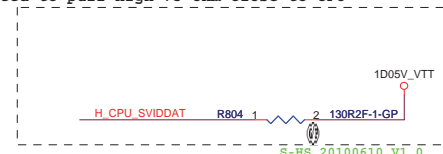
VCCIO Output Decoupling Recommendation:
2 x 330 uF (3 x 330 uF for 2012 capable designs)
5 x 22 uF & 5 x 0805 no-stuff at Bottom
7 x 22 uF & 2 x 0805 no-stuff at Top



No-stuff sites outside the socket may be removed.
No-stuff sites inside the socket cavity need to remain.



For CRB VIDSOUT need to pull high 130 ohm close to CPU and IMVP7
For CRB VIDALERT# need to pull high 75 ohm close to CPU



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

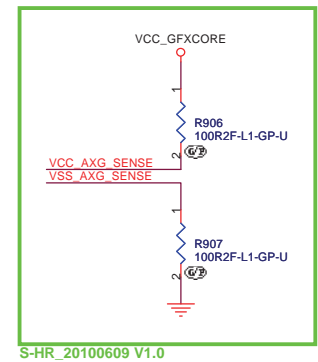
Title
Size Custom
Date: Tuesday, January 18, 2011
CPU (VCC CORE)
Document Number
LLW-1 / LGG-1
Rev
-1
Sheet 8 of 94

SSID = CPU

VAXG Output Decoupling Recommendation:

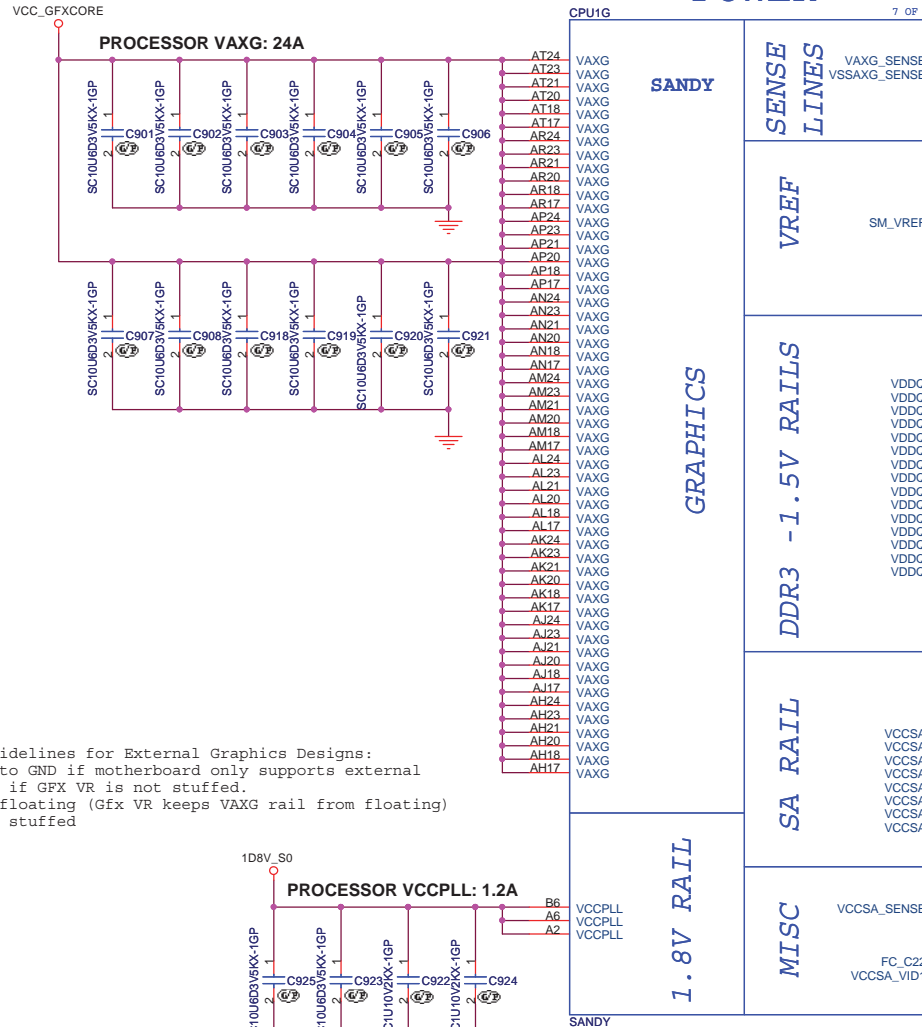
- 2 x 470 uF at Bottom Socket Edge
- 2 x 22 uF at Top Socket Cavity
- 4 x 22 uF at Top Socket Edge
- 2 x 22 uF at Bottom Socket Cavity
- 4 x 22 uF at Bottom Socket Edge

R906,R907 close to CPU



S-HR_20100609 V1.0

POWER



Disabling Guidelines for External Graphics Designs:
Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

VCCPLL Output Decoupling Recommendation:
1 x 330 uF
2 x 1 uF
1 x 10 uF

VAXG_SENSE
VSSAXG_SENSE

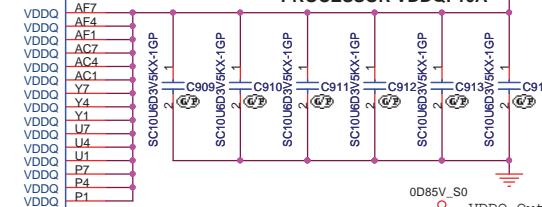
Refer to the latest Huron River Mainstream PDG
(Doc# 436735) for more details on S3 power
reduction implementation.

+V_SM_VREF_CNT should have 10 mil trace width

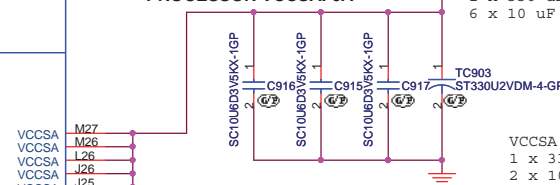
AL1 +V_SM_VREF_CNT << +V_SM_VREF_CNT 37

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT
should have 10 mils trace width.

PROCESSOR VDDQ: 10A



PROCESSOR VCCSA: 6A



VCCSA Output Decoupling Recommendation:
 1 x 330 uF
 2 x 10 uF at Bottom Socket Cavity
 1 x 10 uF at Bottom Socket Edge

R902 need be close to pin H23.

VCCSA_SENSE

FC_C21
VCCSA_VID1

C22	H_FC_C22		H_FC_C22	48
C24	VCCSA_SEL		VCCSA_SEL	48

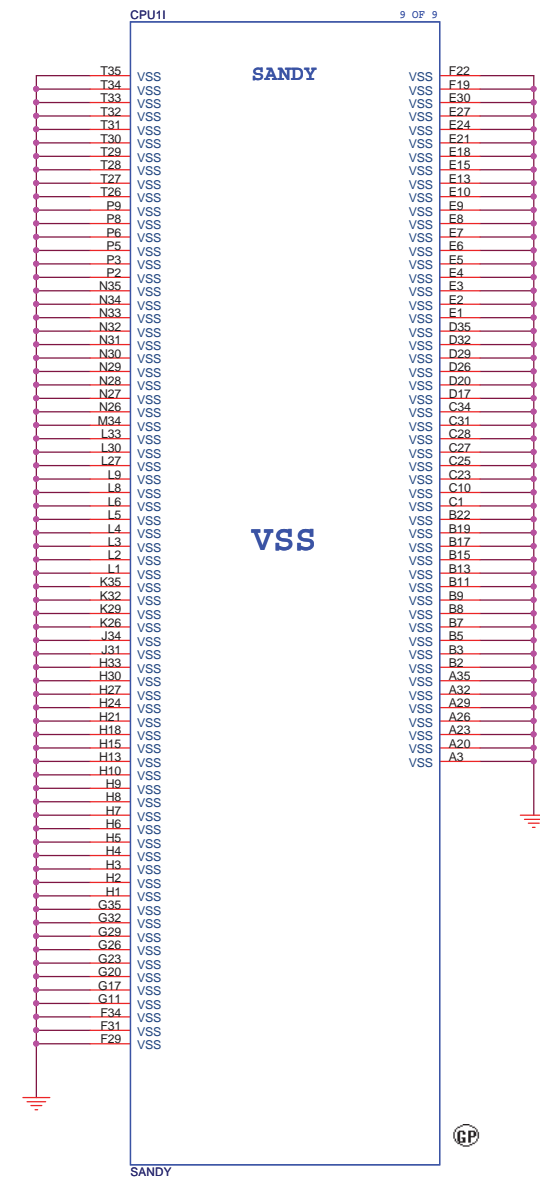
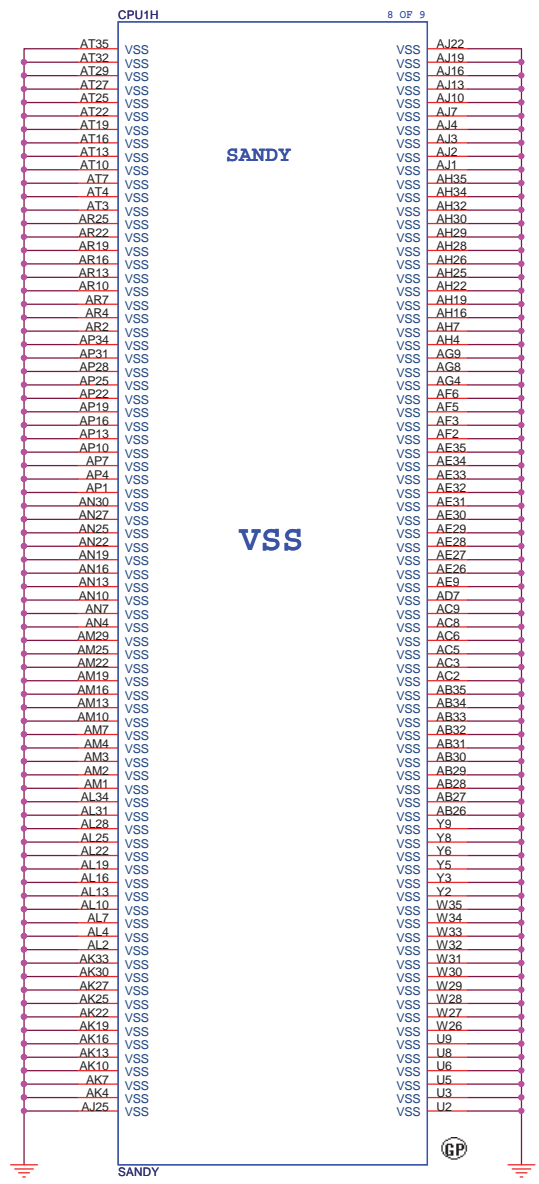
RN901
SRN1KJ-7-GF

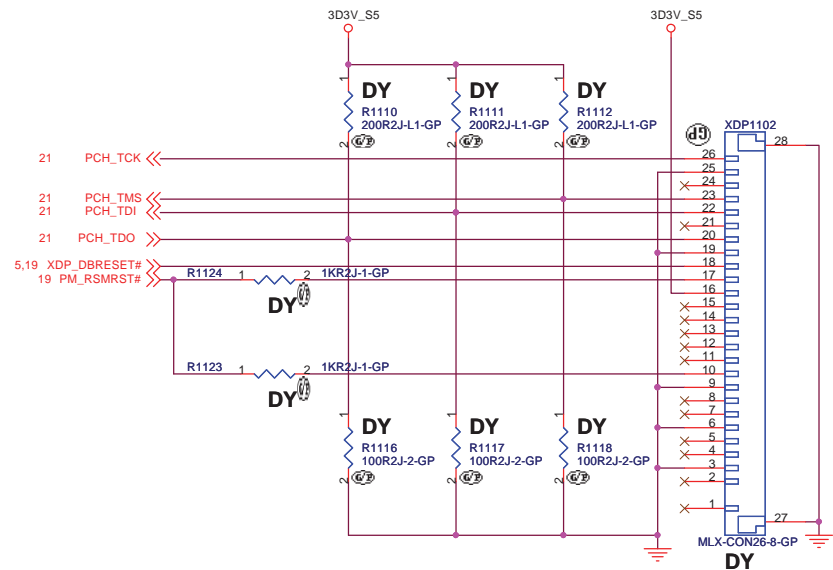
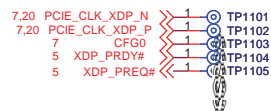
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
CPU (VCC GFXCORE)			
Size A3	Document Number		Rev
	LLW-1 / LGG-1		-1
Date:	Tuesday, January 18, 2011	Sheet 9	of 94

SSID = CPU





DEBUG Interface for Processor.

CPU XDP SFF 26pin IF
Pin 1 OBSFN_A0 (PREQ#, I/O)
Pin 2 OBSFN_A1 (PRDY#, I/O)
Pin 3 GND
Pin 4 OBSDATA_A0 (Open, I/O)
Pin 5 OBSDATA_A1 (Open, I/O)
Pin 6 GND
Pin 7 OBSDATA_A2 (Open, I/O)
Pin 8 OBSDATA_A3 (Open, I/O)
Pin 9 GND
Pin 10 HOOK0 (PWRGD, In)
Pin 11 HOOK1 (BP_PWRGD_RST#, Out)
Pin 12 HOOK2 (CFG0, Out)
Pin 13 HOOK3 (vr_READYSYS_PWROK, Out)
Pin 14 HOOK4 (BCLK, In)
Pin 15 HOOK5 (BCLK#, In)
Pin 16 VCCOBS_AB (VCCP Voltage of CPU, In)
Pin 17 HOOK6 (RESET#, Out)
Pin 18 HOOK7 (DBR#, Out)
Pin 19 GND
Pin 20 TDO, In
Pin 21 TRST#, Out
Pin 22 TDI, Out
Pin 23 TMS, Out
Pin 24 TCK1 (Open)
Pin 25 GND
Pin 26 TCK0 ,Out

TABLE

PCH PIN	REF DES	PCH ES1 JTAG		PCH ES2 JTAG		PRODUCTION	
		Enable	Disable	Enable	Disable	Enable	Disable
TDO	R1110	DY	DY	200 Ohms	DY	DY	DY
	R1116	DY	DY	100 Ohms	DY	DY	DY
	R2	DY	DY	DY	DY	51 Ohms	DY
TMS	R1112	200 Ohms	DY	200 Ohms	DY	DY	DY
	R1118	100 Ohms	DY	100 Ohms	DY	DY	DY
	R91	DY	DY	DY	DY	51 Ohms	DY
TDI	R1111	200 Ohms	20K Ohms	200 Ohms	DY	DY	DY
	R1117	100 Ohms	10K Ohms	100 Ohms	DY	DY	DY
	R90	DY	DY	DY	DY	51 Ohms	DY
TCK	R541	51 Ohms	51 Ohms	51 Ohms	51 Ohms	51 Ohms	51 Ohms
TRST#	R953	20K Ohms	DY	DY	DY	DY	DY
	R535	10K Ohms	DY	DY	DY	DY	DY
	R103	DY	DY	DY	DY	DY	DY

↑
LOGIC

DEBUG Interface for PCH.

PCH XDP SFF 26pin IF
Pin 1 OBSFN_A0 (Open, I/O)
Pin 2 OBSFN_A1 (Open, I/O)
Pin 3 GND
Pin 4 OBSDATA_A0 (Open, I/O)
Pin 5 OBSDATA_A1 (Open, I/O)
Pin 6 GND
Pin 7 OBSDATA_A2 (Open, I/O)
Pin 8 OBSDATA_A3 (Open, I/O)
Pin 9 GND
Pin 10 HOOK0 (RSMRST#, In)
Pin 11 HOOK1 (BP_PWRGD_RST#, Out)
Pin 12 HOOK2 (Open)
Pin 13 HOOK3 (Open)
Pin 14 HOOK4 (Open)
Pin 15 HOOK5 (Open)
Pin 16 VCCOBS_AB (3.3VSUS, In)
Pin 17 HOOK6 (RSMRST#, Out)
Pin 18 HOOK7 (DBR#, Out)
Pin 19 GND
Pin 20 TDO (JTAG, In)
Pin 21 TRST# (Open)
Pin 22 TDI (JTAG, Out)
Pin 23 TMS (JTAG, Out)
Pin 24 TCK1 (Open)
Pin 25 GND
Pin 26 TCK0 (JTAG, Out)

<Core Design>

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
XDP CONN			
Size	Document Number	Rev	
A3	LLW-1 / LGG-1	-1	
Date:	Tuesday, January 18, 2011	Sheet	11 of 94

BLANK

<Core Design>

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
Reserved		
Size	Document Number	Rev
A4	LLW-1 / LGG-1	-1
Date: Tuesday, January 18, 2011		Sheet 12 of 94

BLANK

<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CLOCK GEN

Size
A4

Document Number

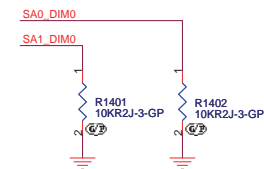
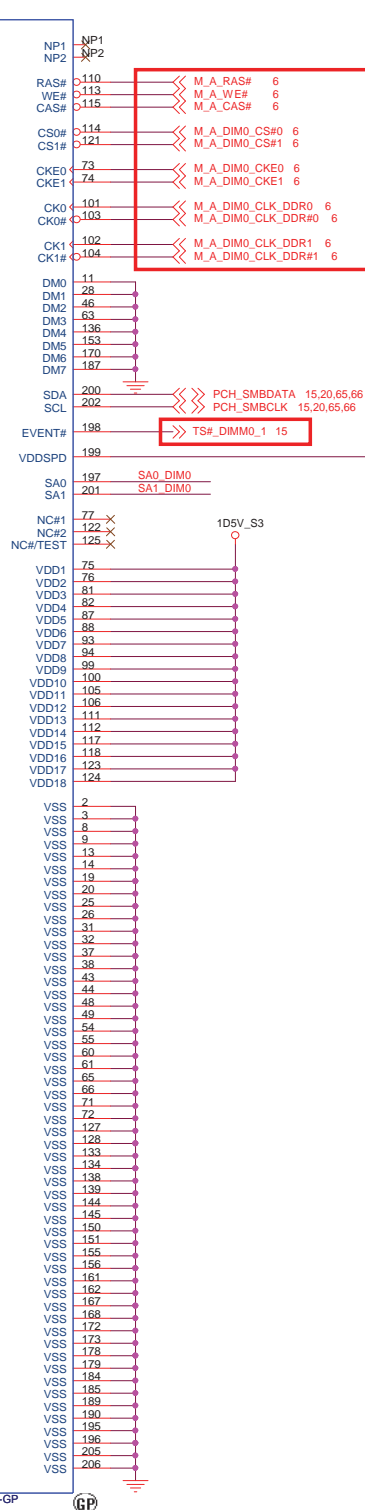
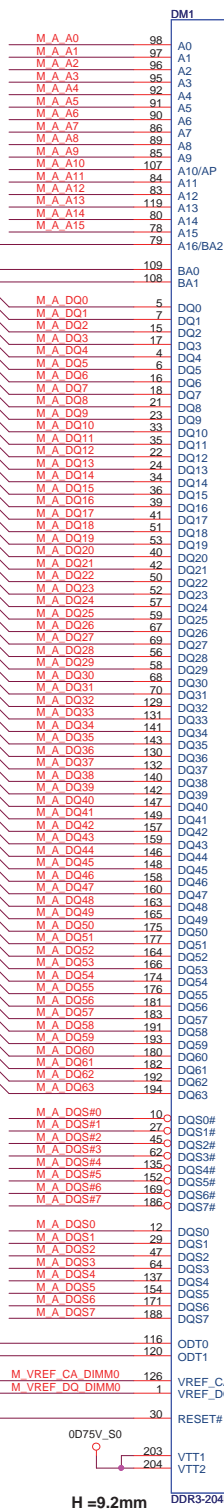
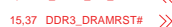
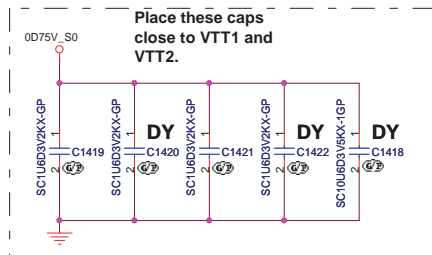
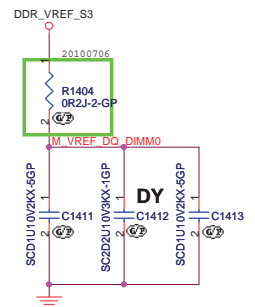
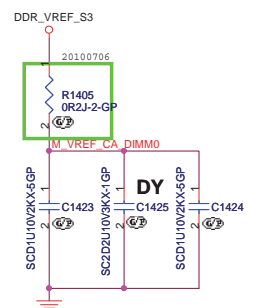
LLW-1 / LGG-1

Rev
-1

Date: Tuesday, January 18, 2011

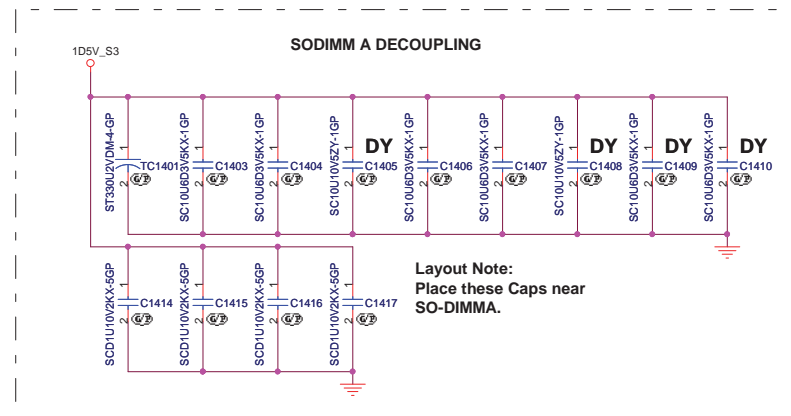
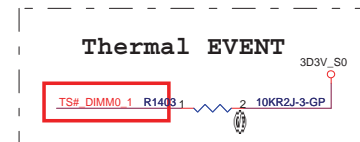
Sheet 13 of 94

SSID = MEMORY



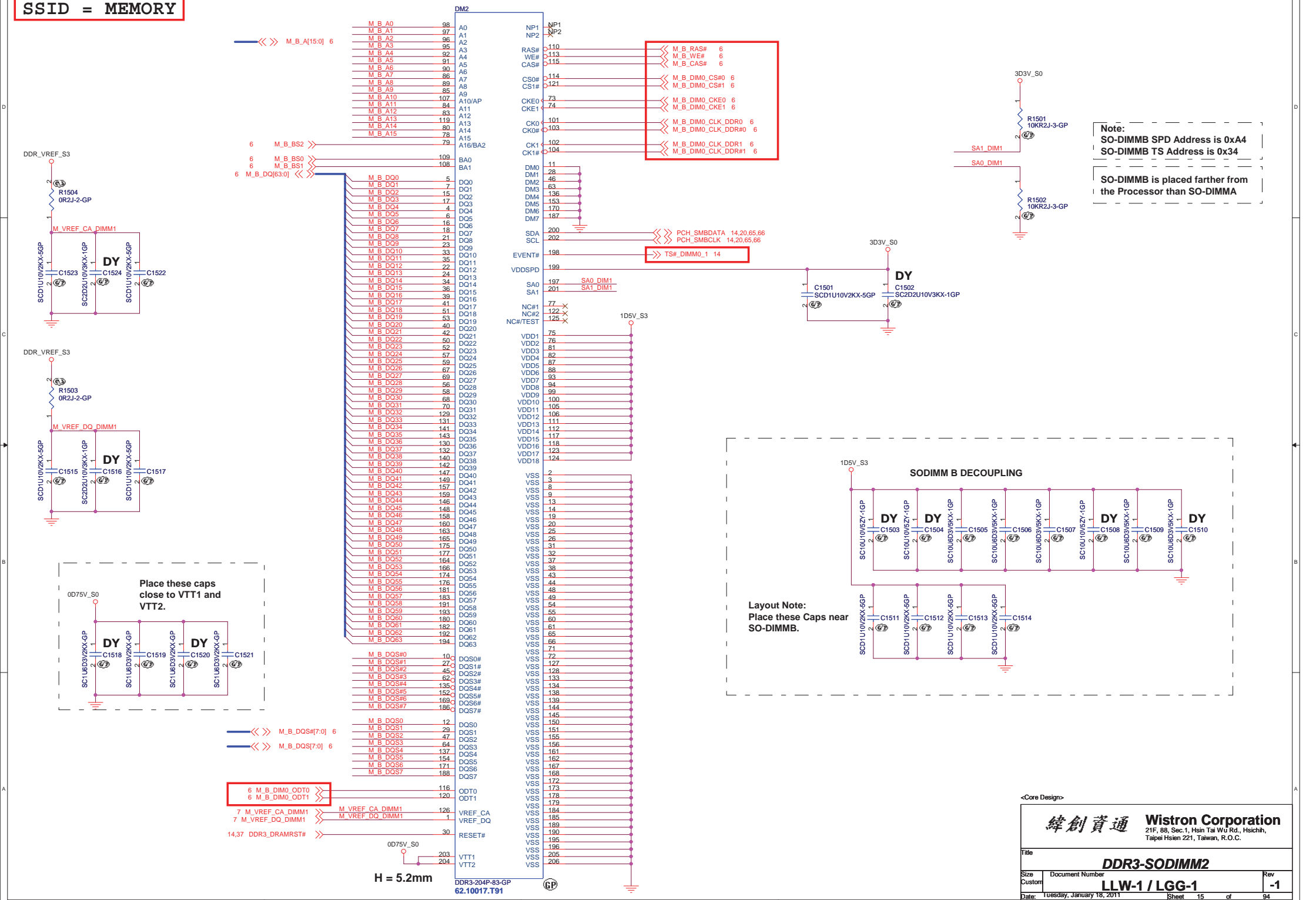
Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32



Layout Note:
Place these Caps near
SO-DIMMA.

SSID = MEMORY

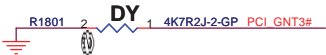
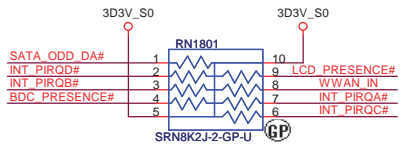


(Blanking)

<Core Design>

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>DDR3-SODIMM2</div>		
Size <div>A4</div>	Document Number <div>LLW-1 / LGG-1</div>	Rev <div>-1</div>
Date: Tuesday, January 18, 2011		Sheet 16 of 94

SSID = PCH

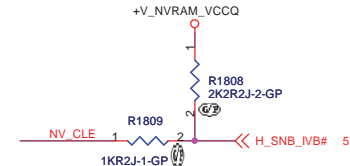
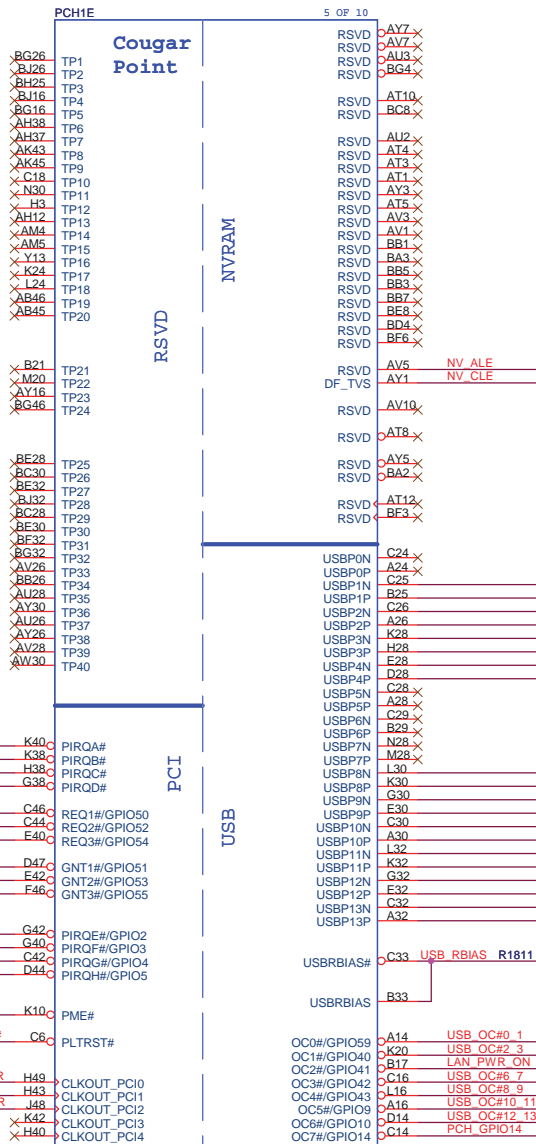
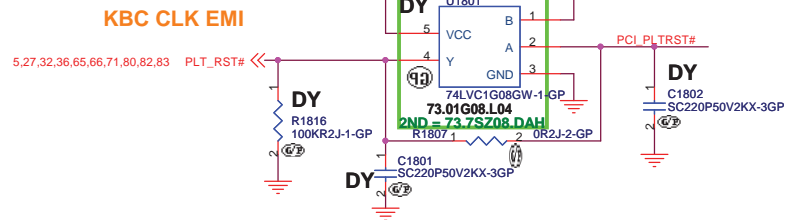
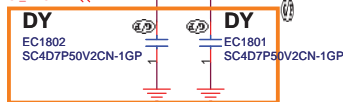
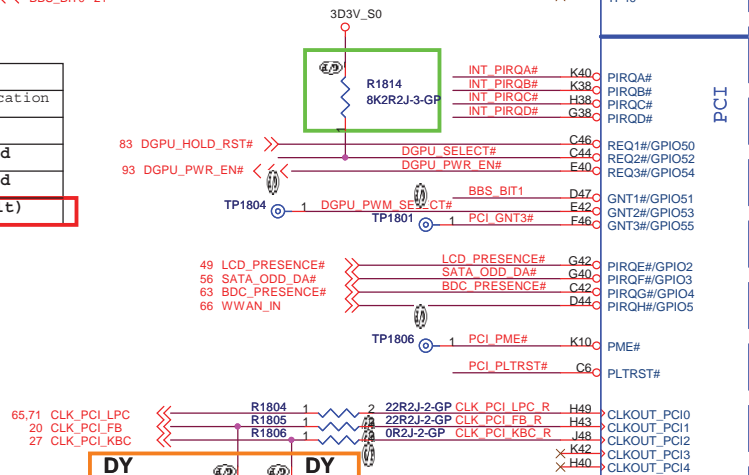
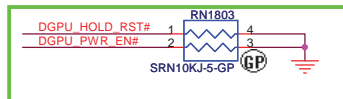
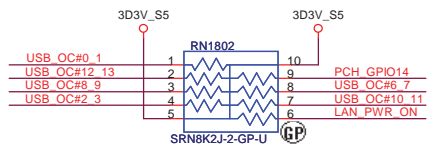


A16 swap override Strap/Top-Block
Swap Override jumper

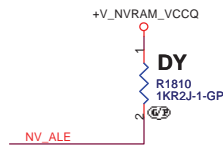
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enable High = Default
-----------	--



BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)



DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH



USB	
Pair	Device
0	X
1	USB2
2	FINGERPRINT
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	X
6	X
7	X
8	ESATA1
9	USB1
10	USB Ext. port 4
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

מחלקת המחקר והפיתוח

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

PCH (PCI/USB/NVRAM)

Size

Document Number

LLW-1 / LGG-1

Rev

Date: Tuesday, January 18, 2011

Sheet 18 of

94

SSID = PCH

4 DMI_RXN[3..0] <<>>=
4 DMI_RXP[3..0] <<>>=
4 DMI_TXN[3..0] <<>>=
4 DMI_TXP[3..0] <<>>=

<<>> FDI_TXN[7..0] 4
<<>> FDI_TXP[7..0] 4

Deep S4/S5 Supported

Deep S4/S5 Not Supported

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and
routing length less than 500
mils.
DMI_IRCOMP keep W=4 mils and
routing length less than 500
mils.

VccDSW3_3

DPWROK

VccSUS3_3

RSMRST#

For platforms not supporting Deep S4/S5

- 1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
- 2.DPWROK and RSMRST# will rise at the same time (connected on board)
- 3.SLP_SUS# and SUSACK# are left as 'no connect'
- 4.SUSWARN# used as SUSWRDNACK/GPIO30

PCH1C

3 OF 10

Cougar
Point

DMI

FDI

System Power Management

COUGAR-GP-U2-NF

FDI_RXN0 BJ14 <<>> FDI_TXN7 4
FDI_RXN1 AY14 <<>> FDI_TXN6 4
FDI_RXN2 BE14 <<>> FDI_TXN5 4
FDI_RXN3 BH13 <<>> FDI_TXN4 4
FDI_RXN4 BJ12 <<>> FDI_TXN2 4
FDI_RXN5 BG10 <<>> FDI_TXN1 4
FDI_RXN6 BG9 <<>> FDI_TXN0 4
FDI_RXN7 <<>> <<>>
FDI_RXP0 <<>> FDI_TXP7 4
FDI_RXP1 <<>> FDI_TXP6 4
FDI_RXP2 <<>> FDI_TXP5 4
FDI_RXP3 <<>> FDI_TXP4 4
FDI_RXP4 <<>> FDI_TXP3 4
FDI_RXP5 <<>> FDI_TXP2 4
FDI_RXP6 <<>> FDI_TXP1 4
FDI_RXP7 <<>> FDI_TXP0 4

FDI_INT AW16 <<>> FDI_INT 4
FDI_FSYNC0 AV12 <<>> FDI_FSYNC0 4
FDI_FSYNC1 BC10 <<>> FDI_FSYNC1 4
FDI_LSYNC0 AV14 <<>> FDI_LSYNC0 4
FDI_LSYNC1 BB10 <<>> FDI_LSYNC1 4

DSWVRMEN A18 DSWODVREN

DPWROK E22 PCH_DPWROK R1911 1 10KR2J-3-GP PM_RSMRST#

WAKE# B9 PCIE_WAKE# <<>> PCIE_WAKE# 65,32

CLKRUN#/GPIO32 N3 PM_CLKRUN# <<>> PM_CLKRUN# 27

SUS_STAT#/GPIO61 G8 PM_SUS_STAT# 1 TP1901 TPAD14-GP

SUSCLK#/GPIO62 N14 SUS_CLK R1913 1 10KR2J-2-GP <<>> PCH_SUSCLK_KBC 27

SLP_S5#/GPIO63 D10 PM_SLP_S5# 1 TP1902 TPAD14-GP

SLP_S4# H4 SLP_S4# R R1914 1 10KR2J-2-GP <<>> PM_SLP_S4# 27,46,82

SLP_S3# F4 SLP_S3# R R1915 1 10KR2J-2-GP <<>> PM_SLP_S3# 27,36,37,47,82

SLP_A# G10 PM_SLP_A# 1 TP1903TPAD14-GP

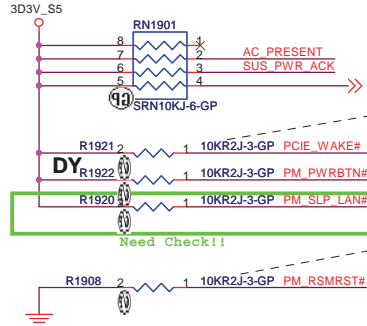
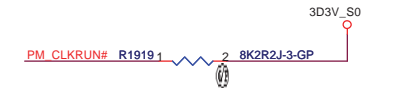
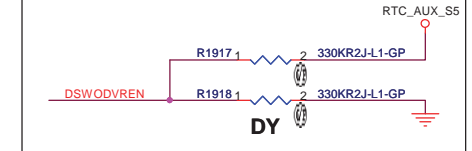
SLP_SUS# G16 PM_SLP_SUS# 1 TP1904TPAD14-GP

PMSYNCH AP14 H_PM_SYNC <<>> H_PM_SYNC 5

SLP_LAN#/GPIO29 K14 PM_SLP_LAN# 1 TP1905TPAD14-GP

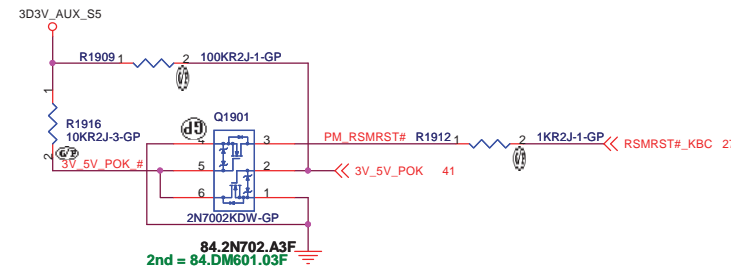
GP

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled



PCIE_WAKE#
CRB : 1K
CEKLT: 10K

PM_RSMRST#
CRB : PL 10K
ANNIE : PL 100K



<Core Design>

緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
PCH (DMI/FDI/PM)	
Size A3	Document Number
LLW-1 / LGG-1	
Date: Tuesday, January 18, 2011	Sheet 19 of 94
Rev -1	

SSID = PCH

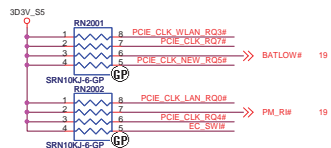
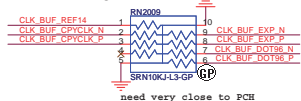
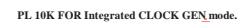
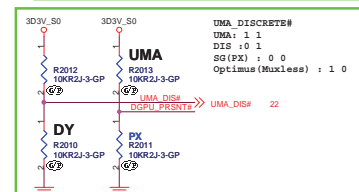
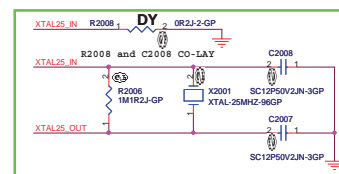
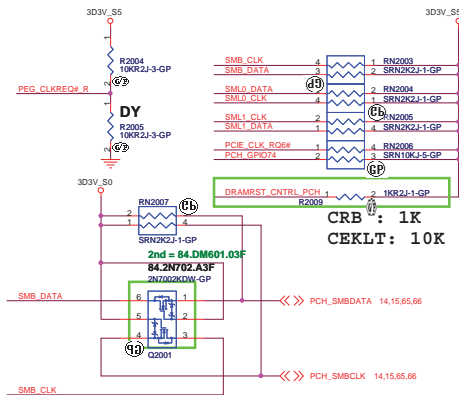
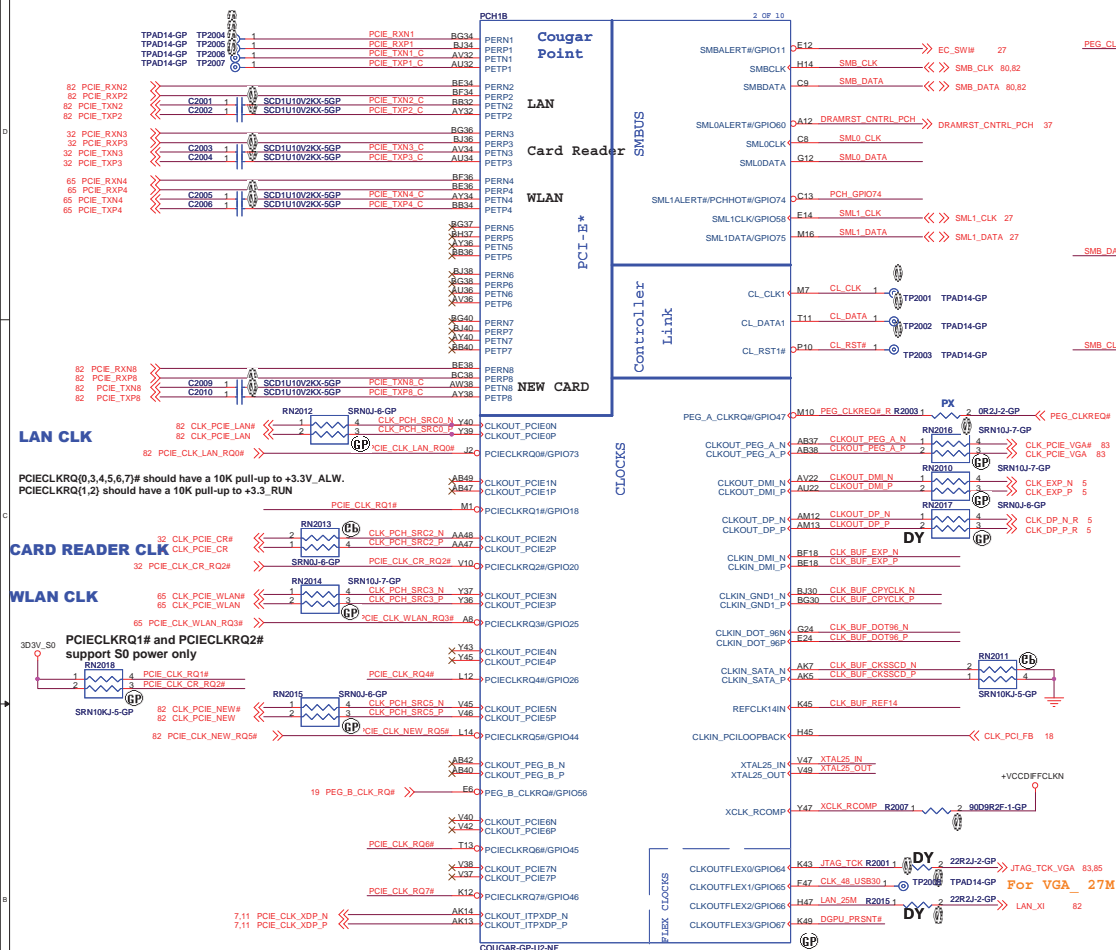


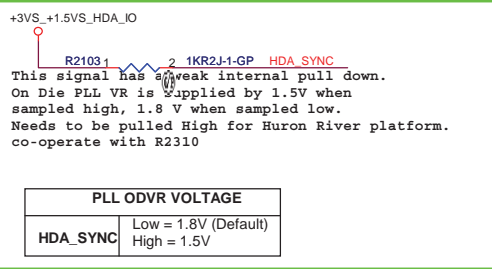
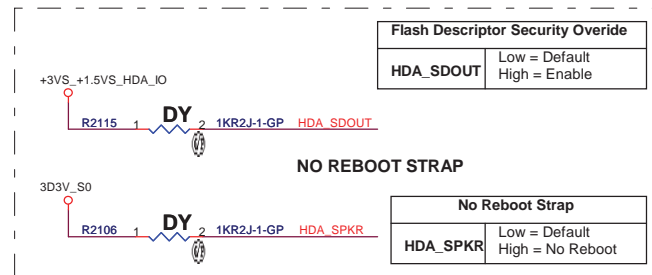
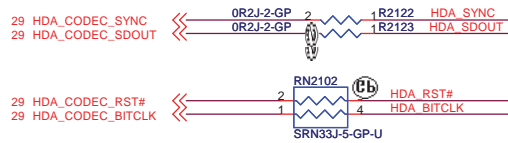
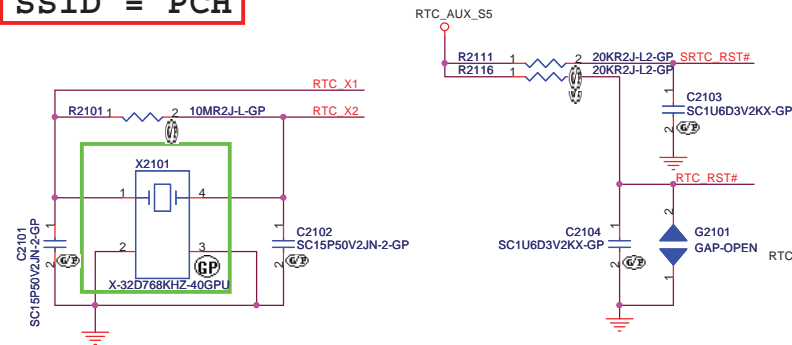
Table 20.1- Dual N-Channel MOSFET multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
PANJIT	2N7002KDW	N/A	84.2N702.A3
DIODES	DMN601DWK-7	N/A	84.DM601.03
NXP	2N7002BKS	N/A	84.2N702.E3

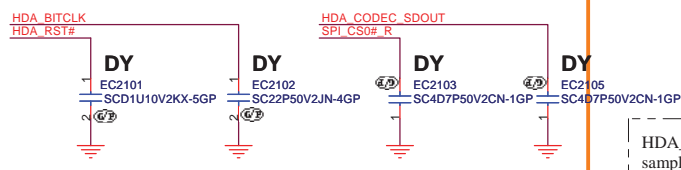
«Core Design:

 緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
PCH (PCI-E/SMBUS/CLOCK/CL)			
Size A2	Document Number		Rev
LLW-1 / LGG-1			
Date:	Tuesday, January 18, 2011	Sheet	20 of 94

SSID = PCH



For EMI



HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVIRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

INTVRMEN- Integrated SUS
1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs

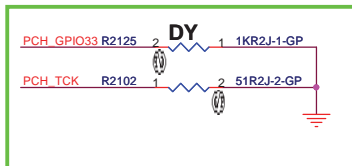
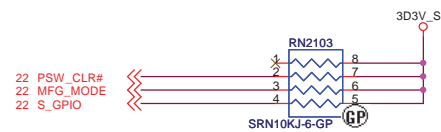
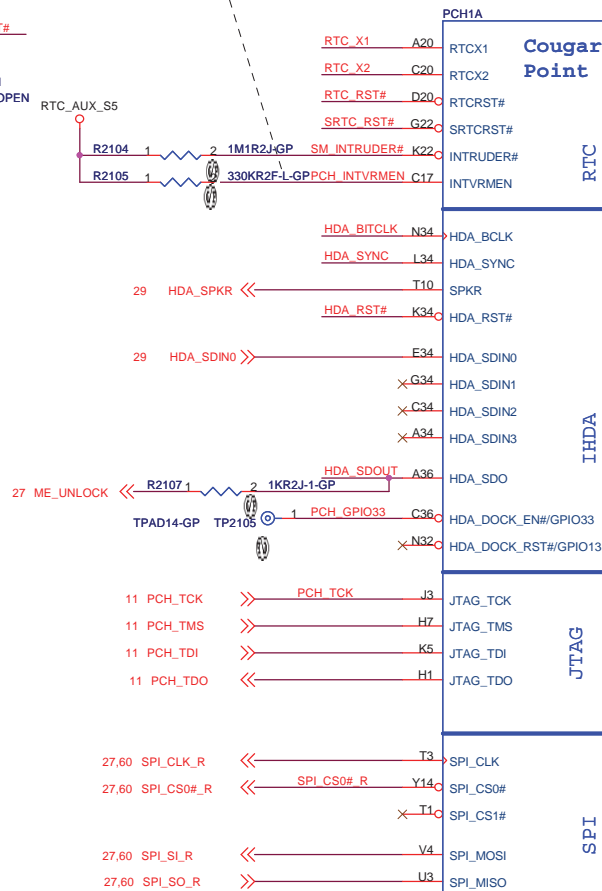
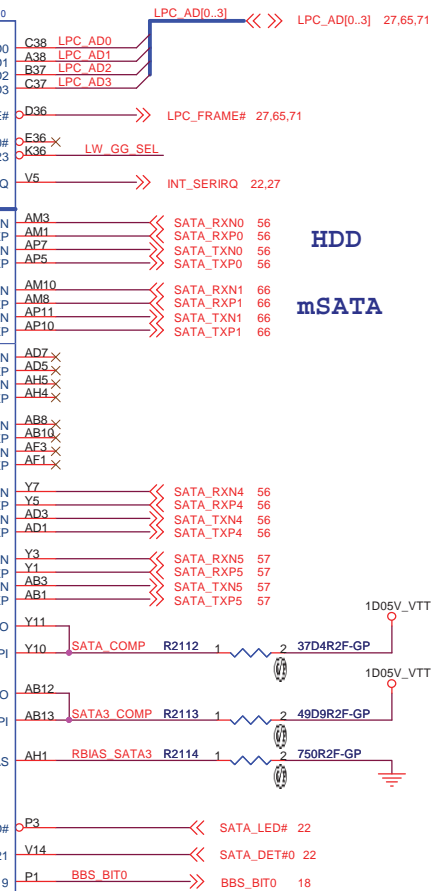
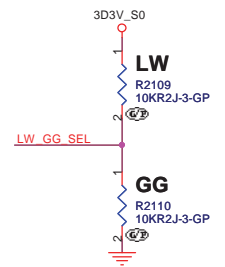


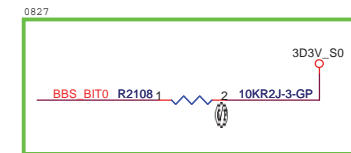
Table 21.1 Project_ID

	LW_GG_SEL
LW	High
GG	LOW



ODD

ESATA



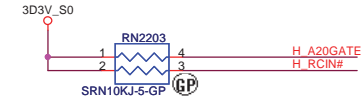
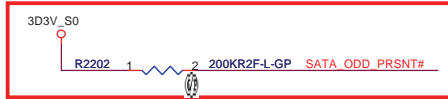
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

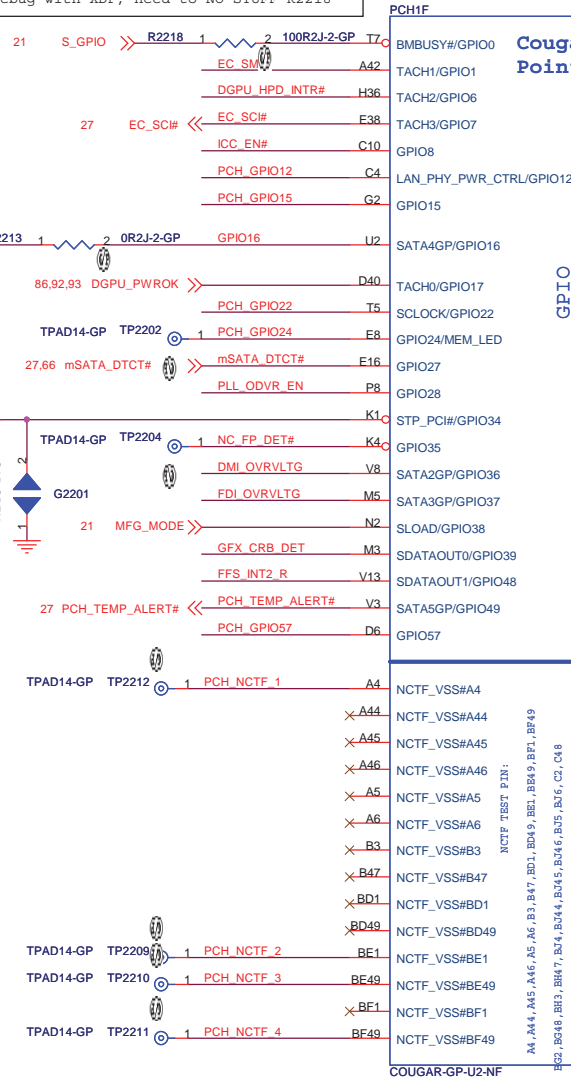
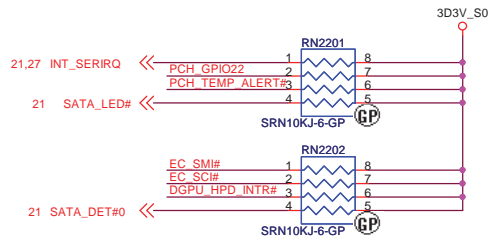
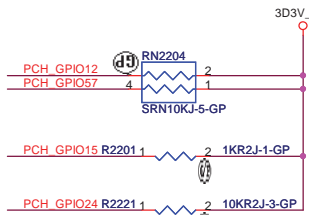
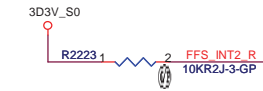
Title			
PCH (SPI/RTC/LPC/SATA/IHDA)			
Size	Document Number		Rev
A3		LLW-1 / LGG-1	-1
Date:	Tuesday, January 18, 2011	Sheet 21 of	94

SSID = PCH

Note:
For PCH debug with XDP, need to NO STUFF R2218



GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regulator,
should not place external pull down.

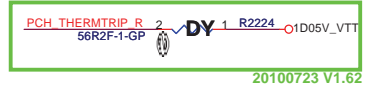
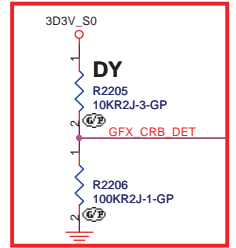
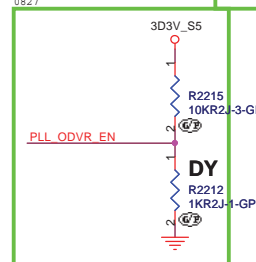
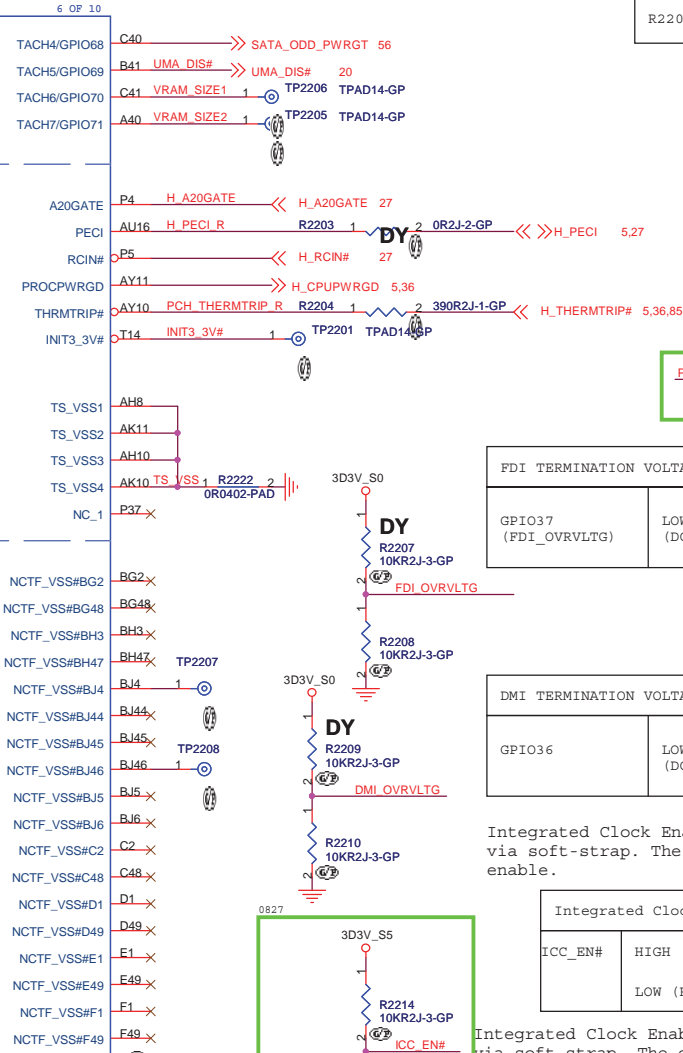


Cougar
Point

GPIO
CPU/MISC

NCTF

COUGAR-GP-U2-NF



FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY) - DISABLED [DEFAULT] LOW (R2211) - ENABLED

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

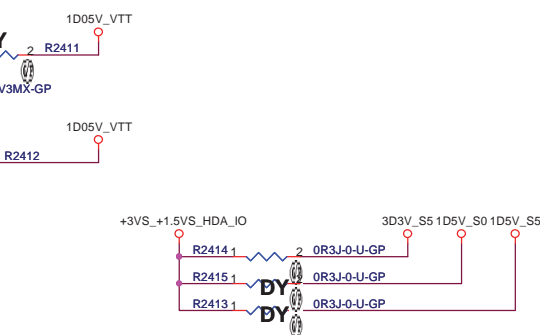
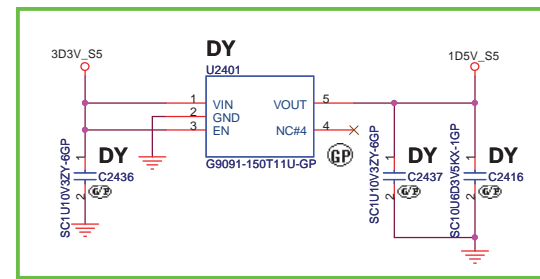
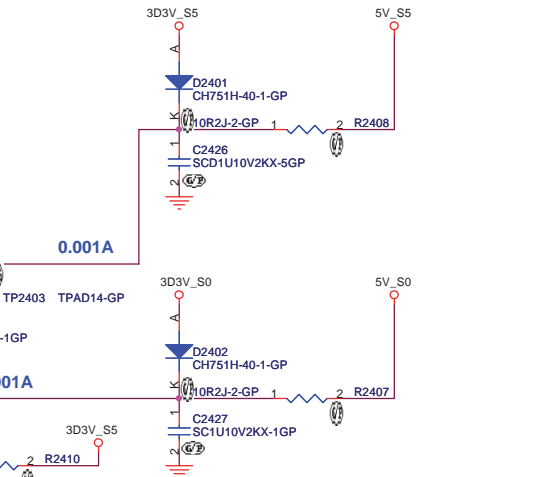
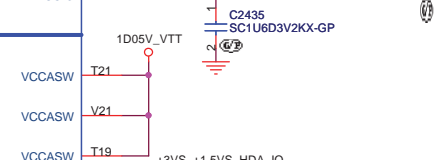
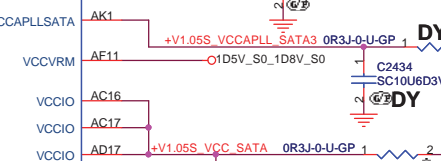
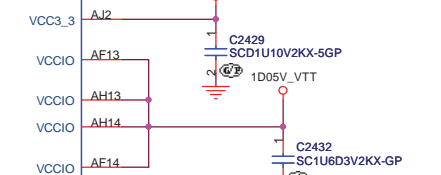
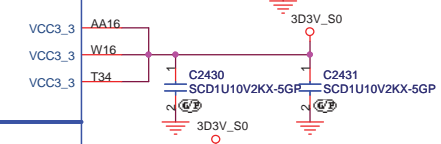
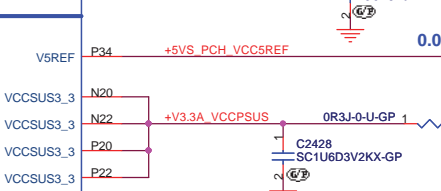
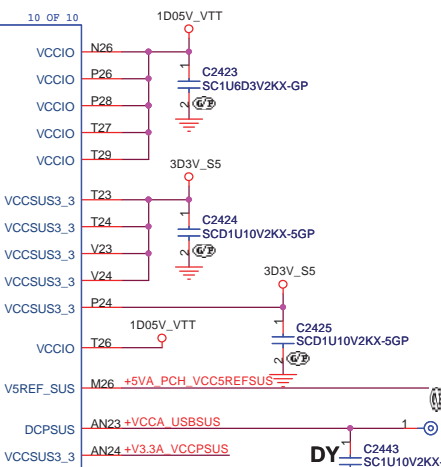
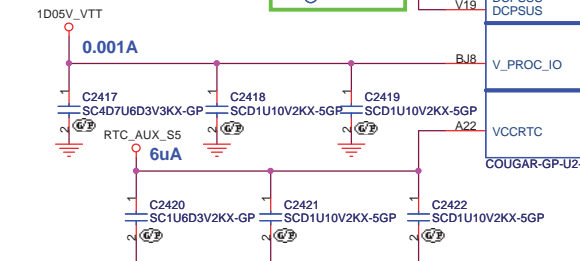
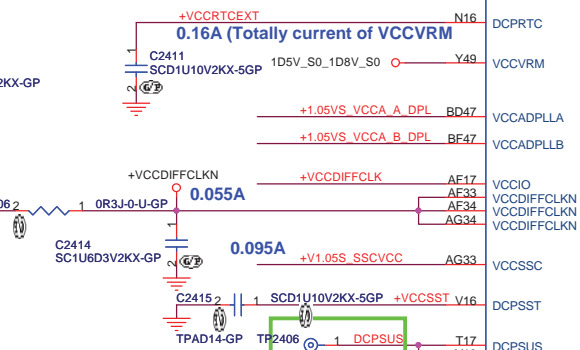
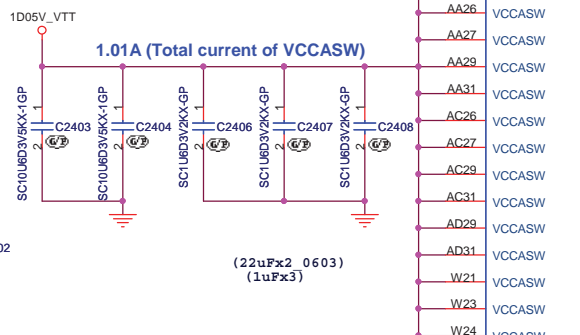
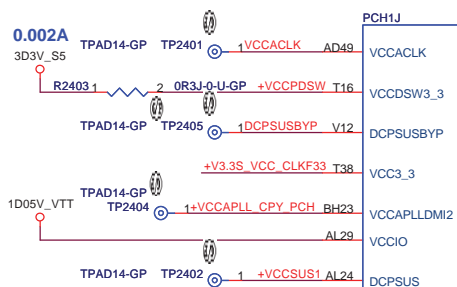
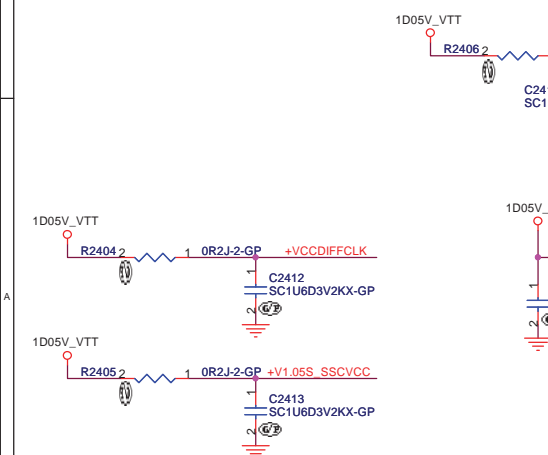
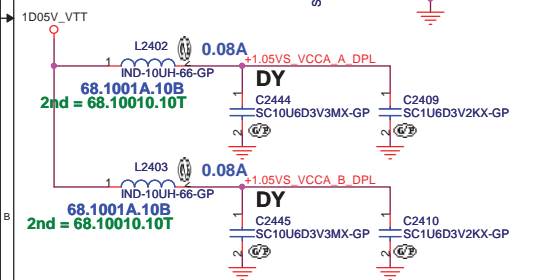
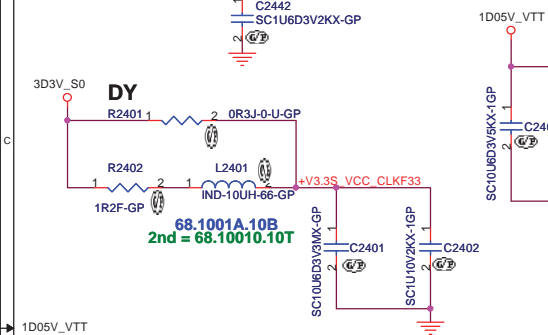
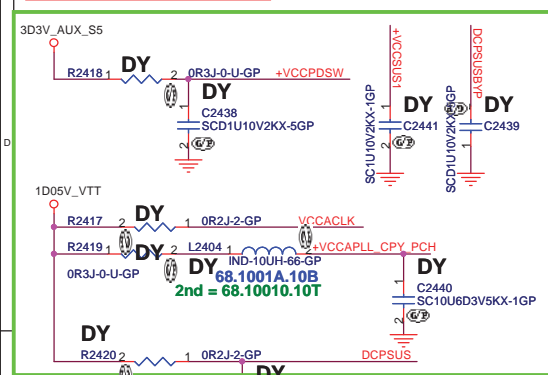
PLL ON DIE VR ENABLE	
ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)	

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		PCH (GPIO/CPU)	
Size	Document Number	LLW-1 / LGG-1	
A3		-1	
Date:	Tuesday, January 18, 2011	Sheet	22 of 94

SSID = PCH

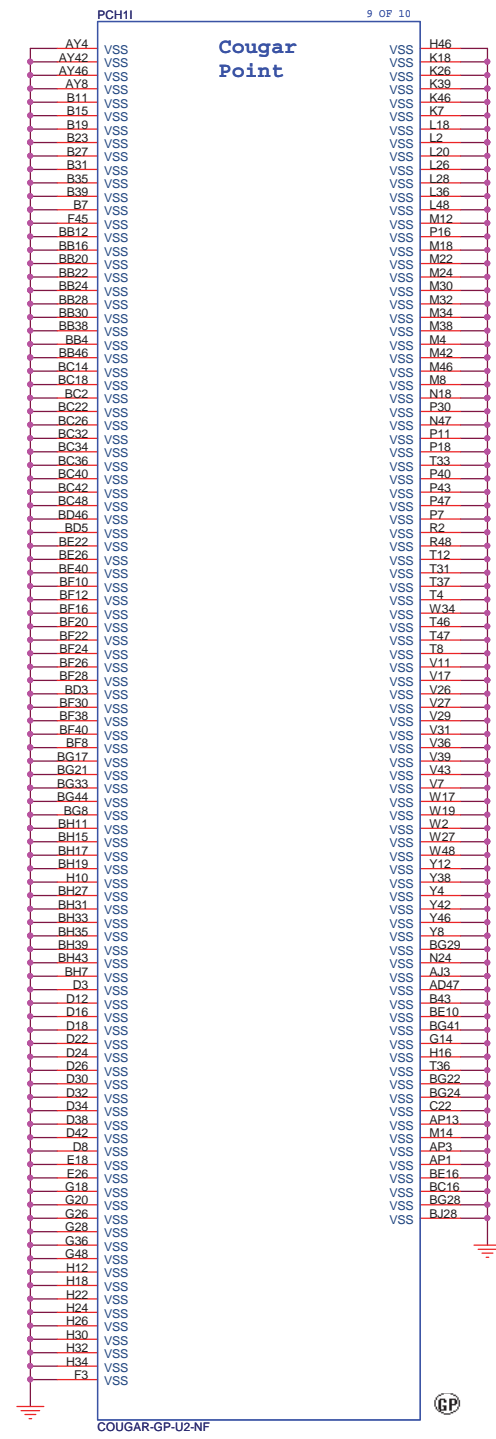
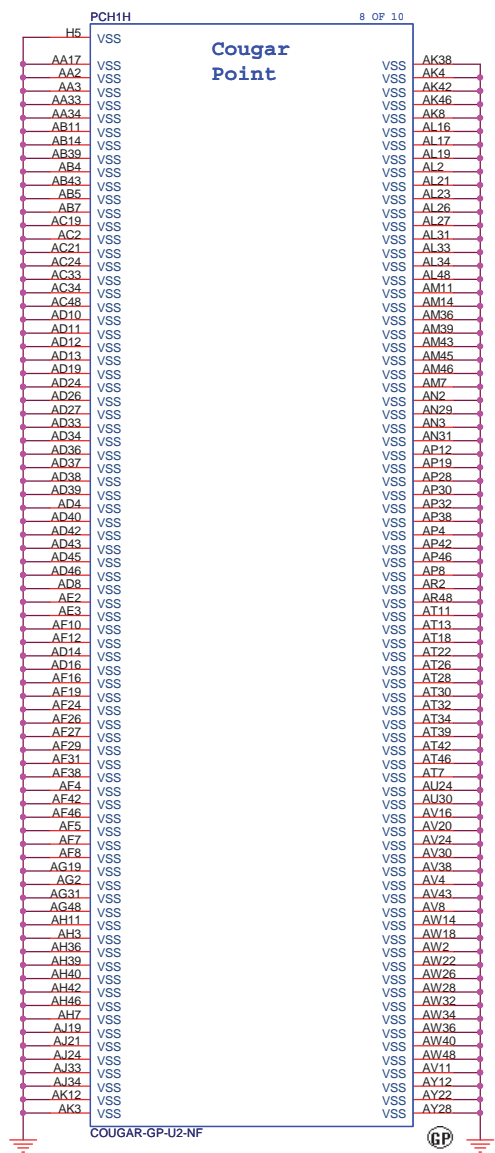


<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
PCH (POWER2)			
Size A3	Document Number		Rev
	LLW-1 / LGG-1		-1
Date: Tuesday, January 18, 2011		Sheet 24 of	94

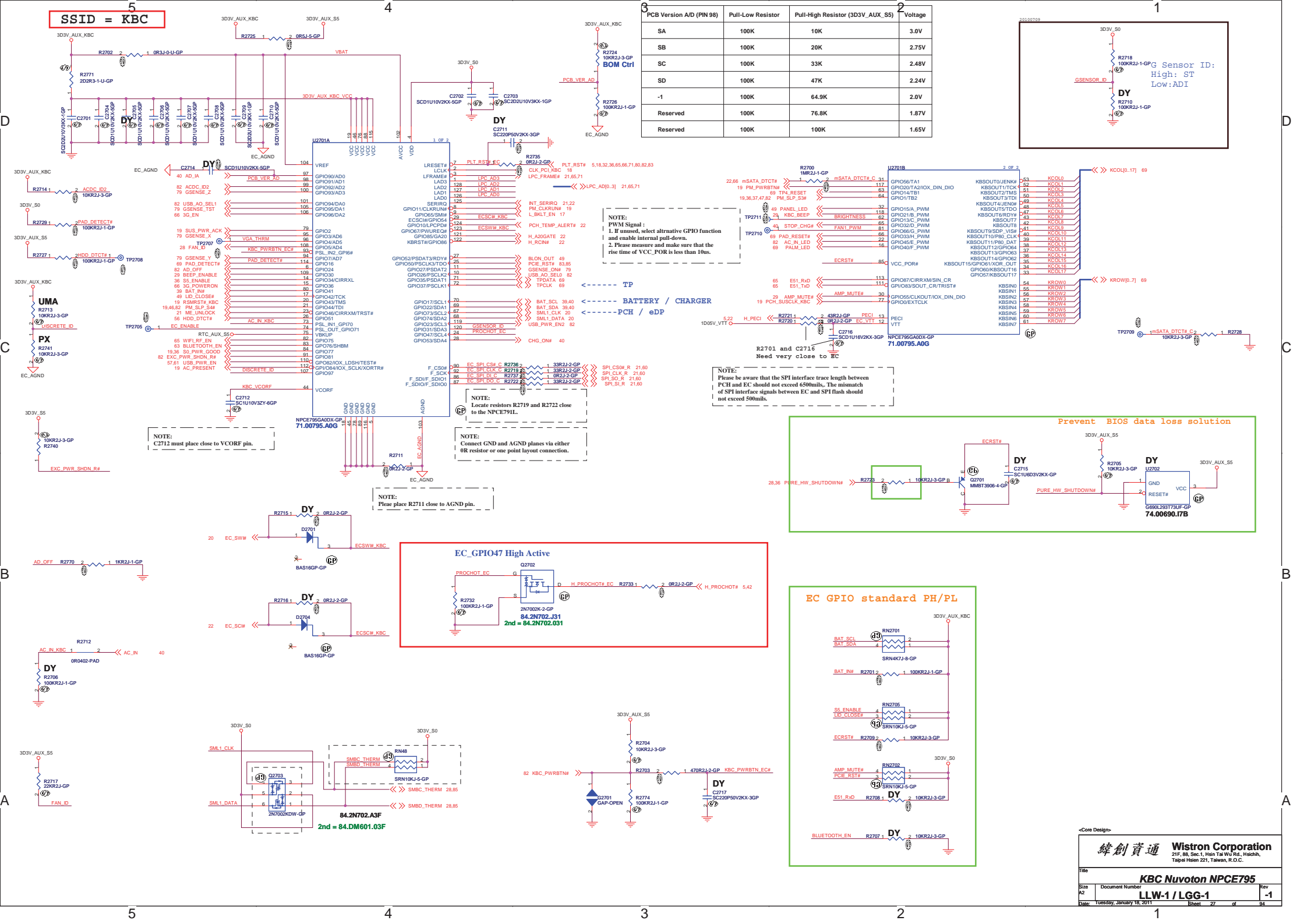
SSID = PCH



BLANK

<Core Design>

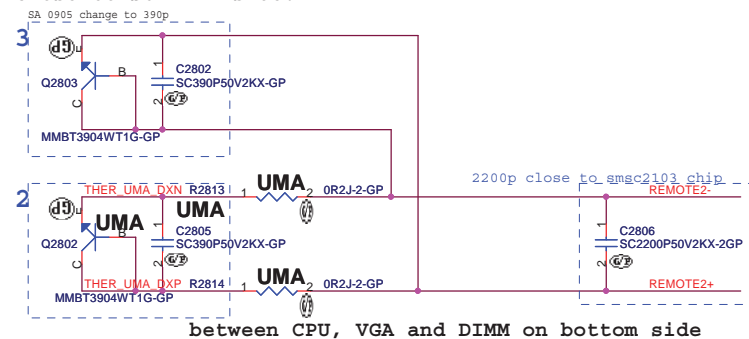
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>LLW-1 / LGG-1</div>	Rev <div>-1</div>
Date: Tuesday, January 18, 2011		Sheet 26 of 94



SSID = Thermal

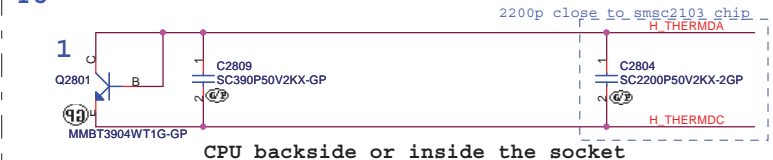
Thermal sensor

Close to SO-DIMM side.



between CPU, VGA and DIMM on bottom side

T8



CPU backside or inside the socket

CPU TEMP:

H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near Thermal diode.

Close to VGA side. PX

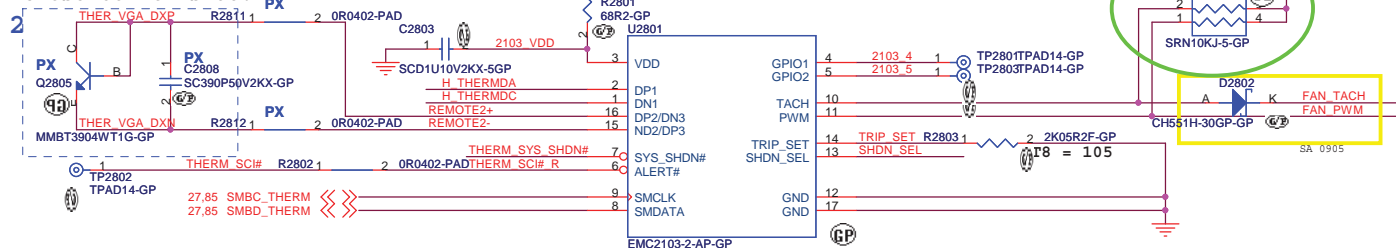
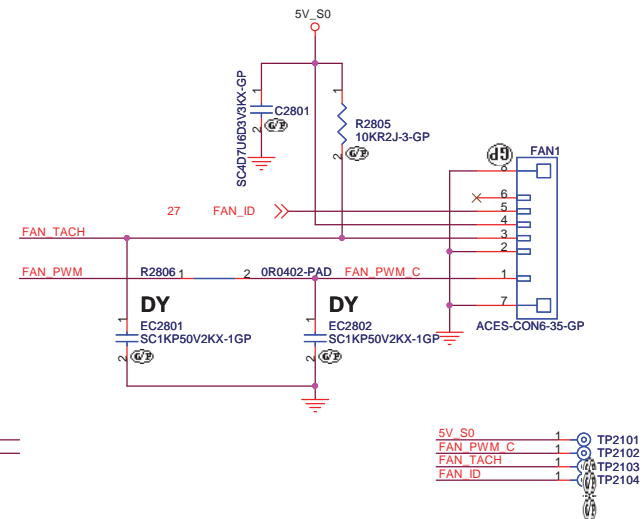
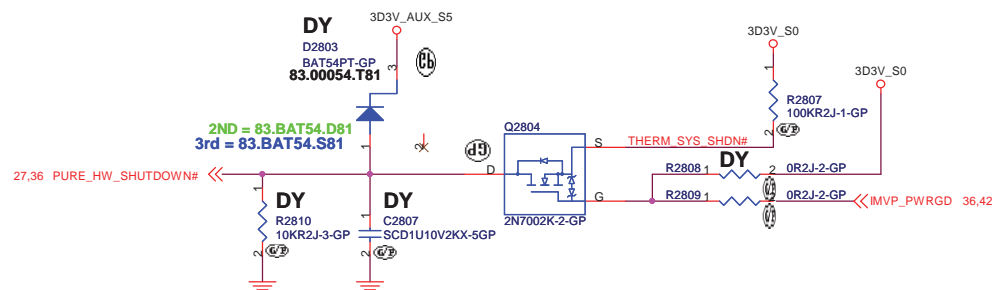
pin6, ALERT# OD
pin7, SYS_SHDN# OD

Table 28.1- General Purpose Transistors multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ON	MMBT3904WT1G	N/A	84.03904.R11
PANJIT	MMBT3904W	N/A	84.M3904.A11
CHENMKO	CH3904WGP	N/A	84.03904.Y11

Table 28.2- Surface Mount Schottky Barrier

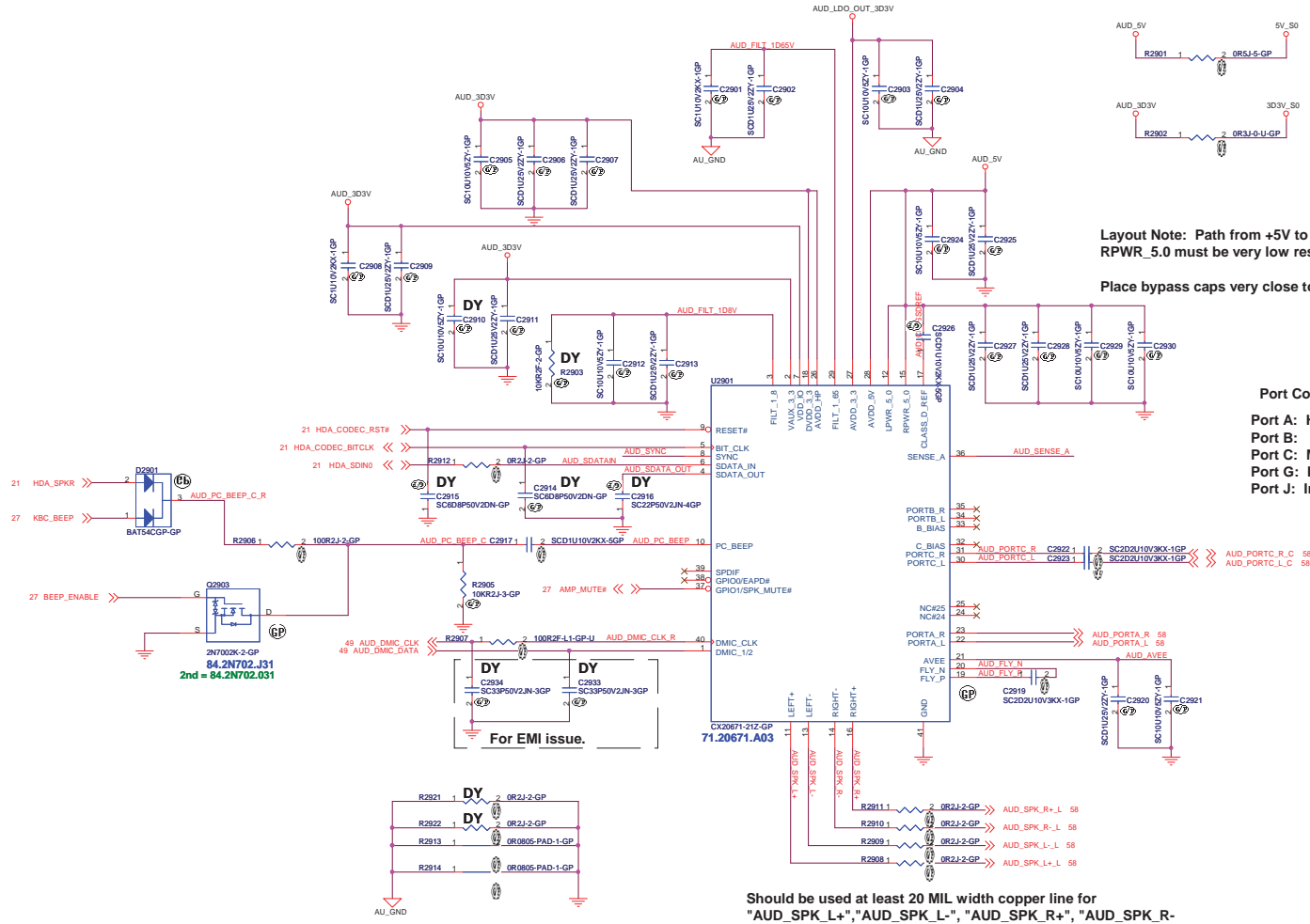
Supplier	Description	Lenovo P/N	Wistron P/N
CHENMKO	BAT54PT	N/A	83.00054.T81
PANJIT	BAT54	N/A	83.BAT54.D81
Power Silicon Inc.	BAT54C	N/A	83.BAT54.S81

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Document Number	Rev
THERMAL SENSOR SMSC EMC2103	LLW-1 / LGG-1	-1
Size A3	Date: Tuesday, January 18, 2011	Sheet 28 of 94

AUDIO CODEC



Layout Note: Path from +5V to LPWR_5.0 and RPWR_5.0 must be very low resistance (<0.01 ohms).

Place bypass caps very close to device.

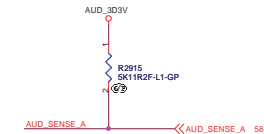
Port Configuration

- Port A: Headphone jack
- Port B:
- Port C: Microphone jack
- Port G: Internal stereo speakers
- Port J: Internal stereo digital mic

JACK DETECT RESISTORS

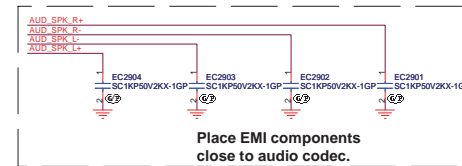
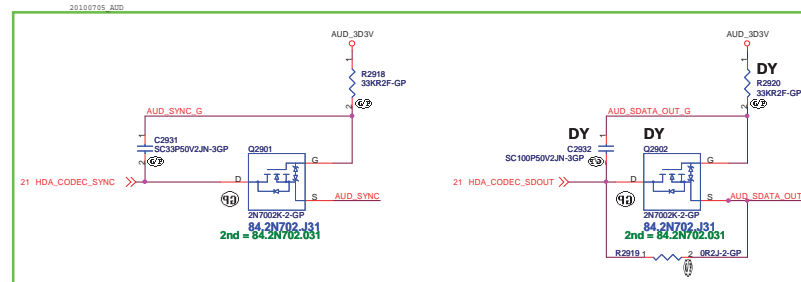
Close to Pin36

SENSE PIN A



Should be used at least 20 MIL width copper line for "AUD_SPK_L+", "AUD_SPK_L-", "AUD_SPK_R+", "AUD_SPK_R-"

Place R2913/R2914 under CODEC, and place R2921/R2922 near CODEC



<Core Design>

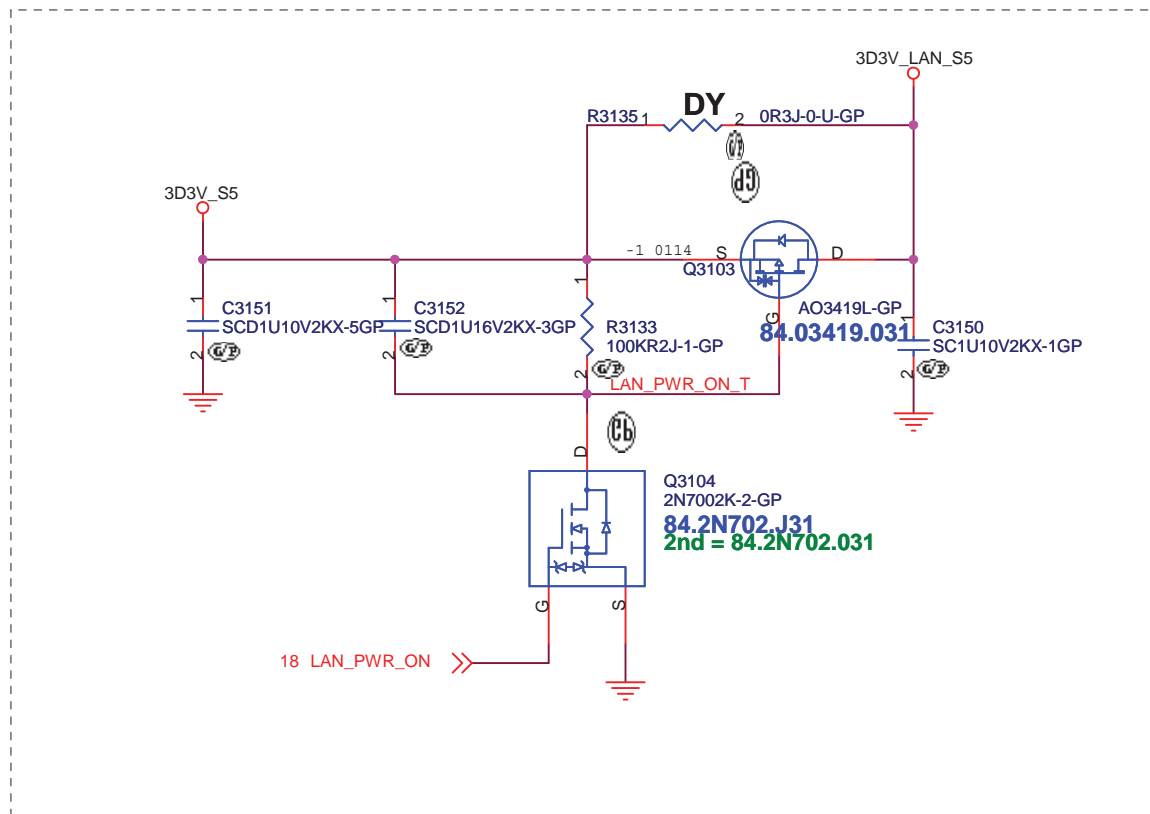
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichia, Taipei Hsien 221, Taiwan, R.O.C.

AUDIO CODEC		
File	Document Number	Rev
LLW-1 / LGG-1		-1
Date: Tuesday, January 16, 2011	Sheet 29	of 94

5	4	3	2	1
D				
C				
B				
A				

<Core Design>

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
AMP		
Size	Document Number	Rev
A3	LLW-1 / LGG-1	-1
Date:	Tuesday, January 18, 2011	Sheet 30 of 94



<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

LAN PWR SW

Size
A4

Document Number

LLW-1 / LGG-1

Rev
-1

Date: Tuesday, January 18, 2011

Sheet 31 of 94

Please place these capacitors, for PCIE_VOUT as close to R5U220 as possible.

Please place these capacitors for VCC_3Vx as close to R5U220 as possible

Please apply wide trace for MF_VOUT between R5U220 and SD Card Slot.
- 2A (W=2mm) Recommended.
- Please consider the number of vias when layer of MF_VOUT is changed.

Please apply external parts, R456, C457, R415 for RXC, CPO, and RREF, as close as possible to R5U220.

Please place these capacitors, for PCIE_VIN as close to R5U220 as possible.

RICOH recommends strongly, Trace length Difference among these SDXC signals are smaller than 0.5 inches.
MDIF_05, SD_CLK MDIF_08, SD_CMD
MDIF_02, SD_DATA0 MDIF_01, SD_DATA1
MDIF_11, SD_DATA2 MDIF_10, SD_DATA3

RICOH recommends strongly, the trace length for these SDXC signals are less than 6-inches.
MDIF_05, SD_CLK MDIF_08, SD_CMD
MDIF_02, SD_DATA0 MDIF_01, SD_DATA1
MDIF_11, SD_DATA2 MDIF_10, SD_DATA3

Please apply capacitor C3210 for SD18C as close as possible to R5U220.

Please apply 50 ohm impedance control for these SDXC signals;
MDIF_05, SD_CLK MDIF_08, SD_CMD
MDIF_02, SD_DATA0 MDIF_01, SD_DATA1
MDIF_11, SD_DATA2 MDIF_10, SD_DATA3

Please use Microstrip trace routing for these SDXC signals
MDIF_05, SD_CLK MDIF_08, SD_CMD
MDIF_02, SD_DATA0 MDIF_01, SD_DATA1
MDIF_11, SD_DATA2 MDIF_10, SD_DATA3

MEDIA I/F	SD/MMC	MEMORYSTICK	XD
MFIO00	SDWP#	MSBS	XD_D7
MFIO01	SD_D1		XD_D6
MFIO02	SD_D0	MS_D1	XD_D5
MFIO03	(SD_D7)		XD_D4
MFIO04	(SD_D6)	(MS_D5)	XD_D3
MFIO05	SD_CLK	MSD0	XD_D2
MFIO06			XD_D1
MFIO07	(SD_D5)	(MS_D4)	XD_D0
MFIO08	SD_CDM	MS_D2	XD_WP#
MFIO09	(SD_D4)	(MS_D6)	XD_WE#
MFIO10	SD_D3	MS_D3	XD_ALE
MFIO11	SD_D2		XD_CLE
MFIO12			XD_CE#
MFIO13		(MS_D7)	XD_RE#
MFIO14		MS_CLK	XD_R/B
MFCD0#	SDDC#		XDCD0#
MFCD1#		MSINS#	XDCD1#

<Core Design>

BLANK

<Core Design>

<div>緯創資通</div>		<div>Wistron Corporation</div>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
1394			
Size A4	Document Number LLW-1 / LGG-1		Rev -1
Date:	Tuesday, January 18, 2011	Sheet 33 of	94

BLANK

<Core Design>

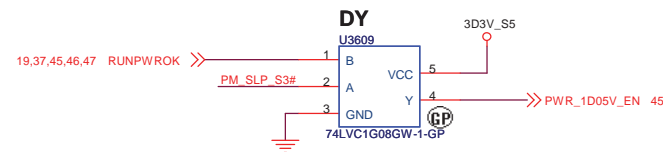
<div>緯創資通</div>		<div>Wistron Corporation</div>	
		<div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
<div>Title</div> <div>Smart Card Reader</div>			
<div>Size</div> <div>A4</div>	<div>Document Number</div> <div>LLW-1 / LGG-1</div>		<div>Rev</div> <div>-1</div>
<div>Date: Tuesday, January 18, 2011</div>		<div>Sheet</div> <div>34</div>	<div>of</div> <div>94</div>

BLANK

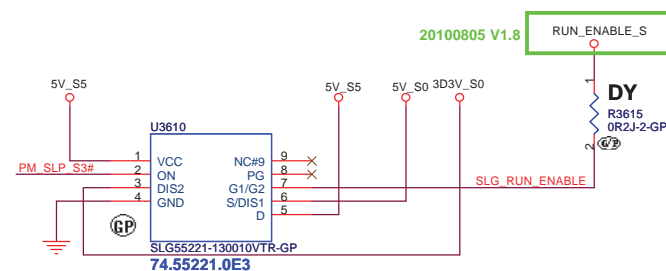
<Core Design>

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title <div>USB3.0</div>		
Size <div>A4</div>	Document Number <div>LLW-1 / LGG-1</div>	Rev <div>-1</div>
Date: Tuesday, January 18, 2011		Sheet 35 of 94

Power Sequence



Run Power



<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

POWER SEQUENCE

Size
A3

Document Number

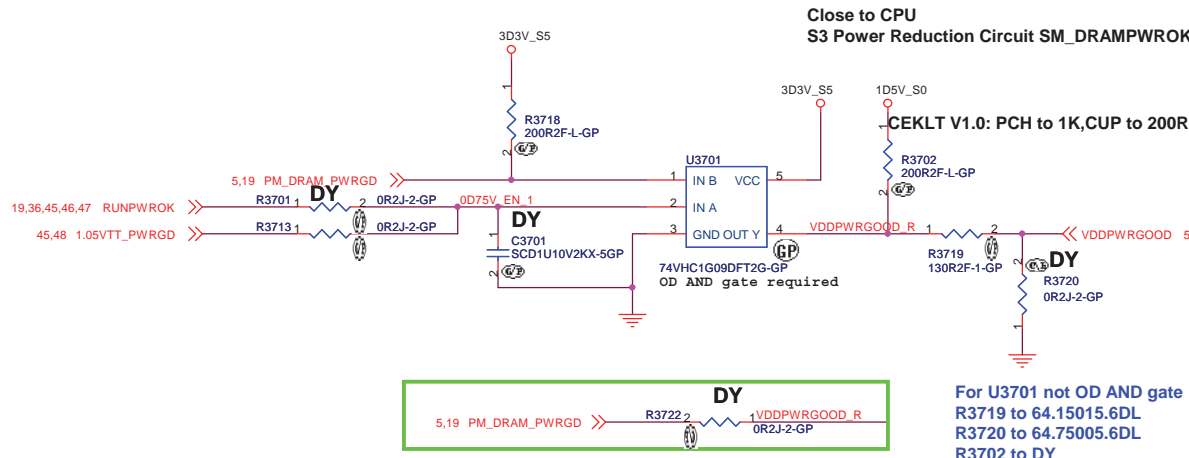
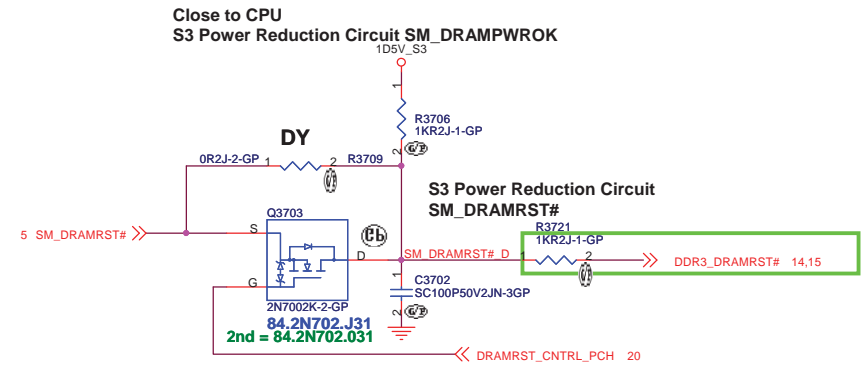
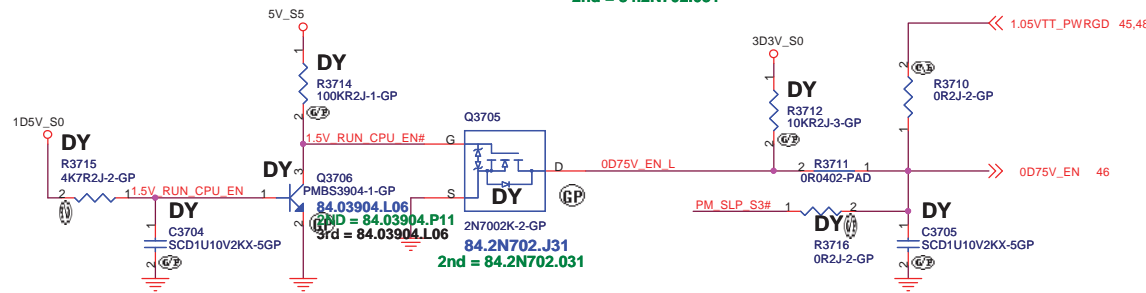
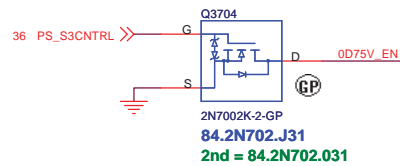
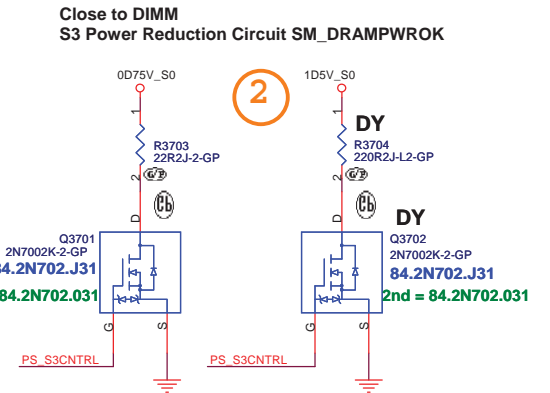
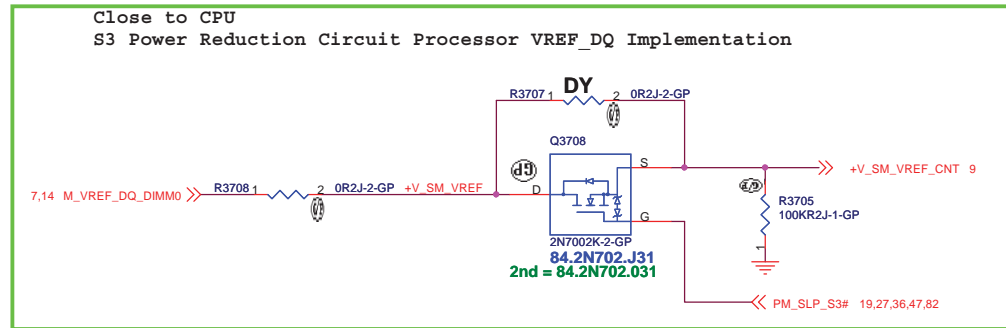
LLW-1 / LGG-1

Rev

Date: Tuesday, January 18, 2011

Sheet	3
-------	---

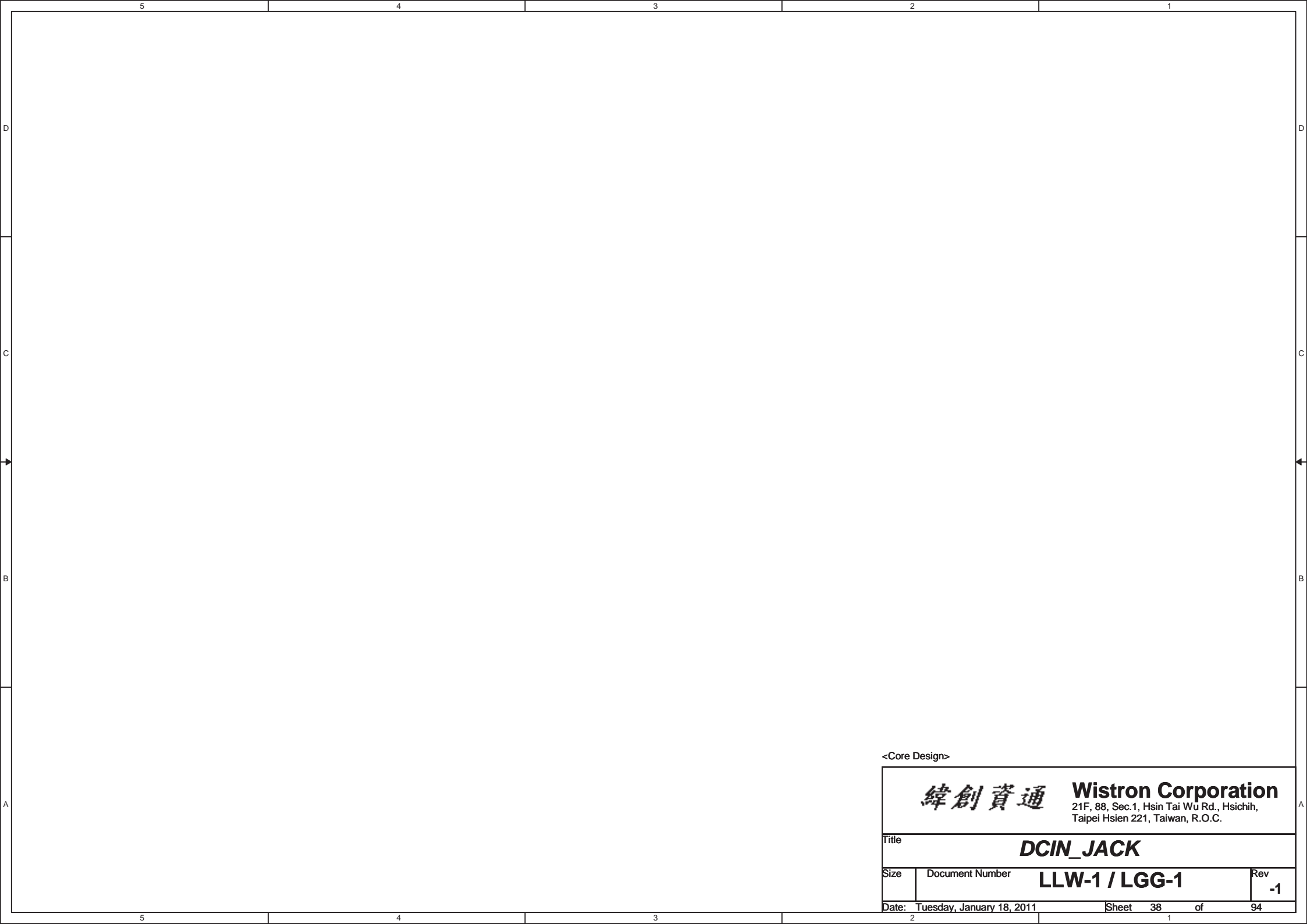
94



SM_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ * 0.55± 200mV and the edge must be monotonic

For U3701 not OD AND gate
R3719 to 64.15015.6DL
R3720 to 64.75005.6DL
R3702 to DY

<Core Design>



<Core Design>

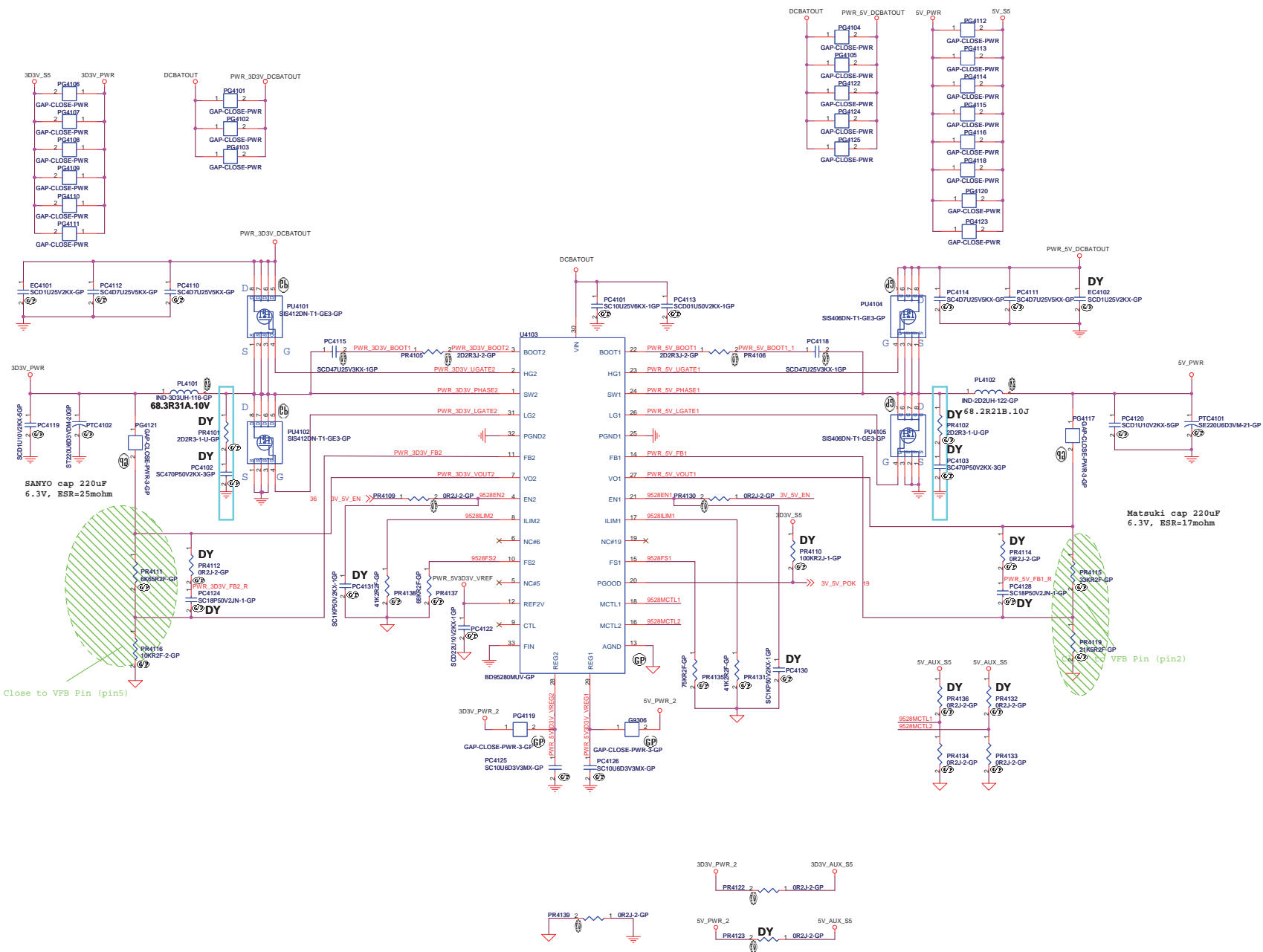


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
<i>DCIN_JACK</i>		

Size	Document Number	Rev
	LLW-1 / LGG-1	-1


```
SSID = PWR.Plane.Regulator_5v3p3v
```



Supplier	Description	Lenovo P/N	Wistron P/N
SANYO	6TPE220MAP	N/A	77.22271.27L
NEC-TOKIN	V0J227M(25)12RE	N/A	77.C2271.00L

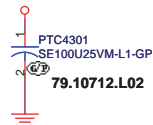
Supplier	Description	Lenovo P/N	Wistron P/N
SANYO	6TPE220MAP	N/A	77.22271.27L
NEC-TOKIN	V0J227M(25)12RE	N/A	77.C2271.00L

◀Core Design▶

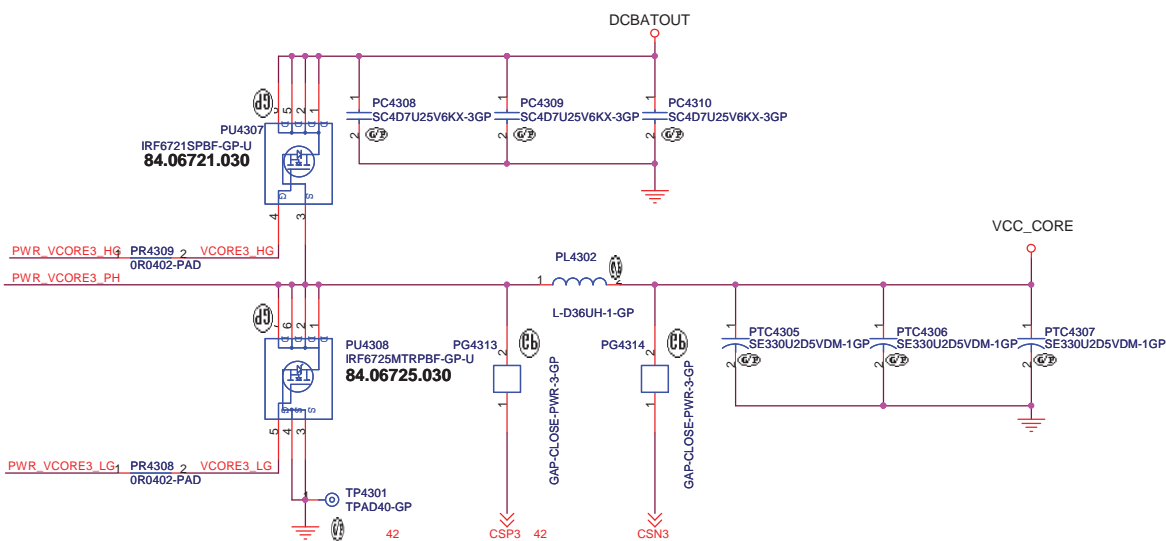
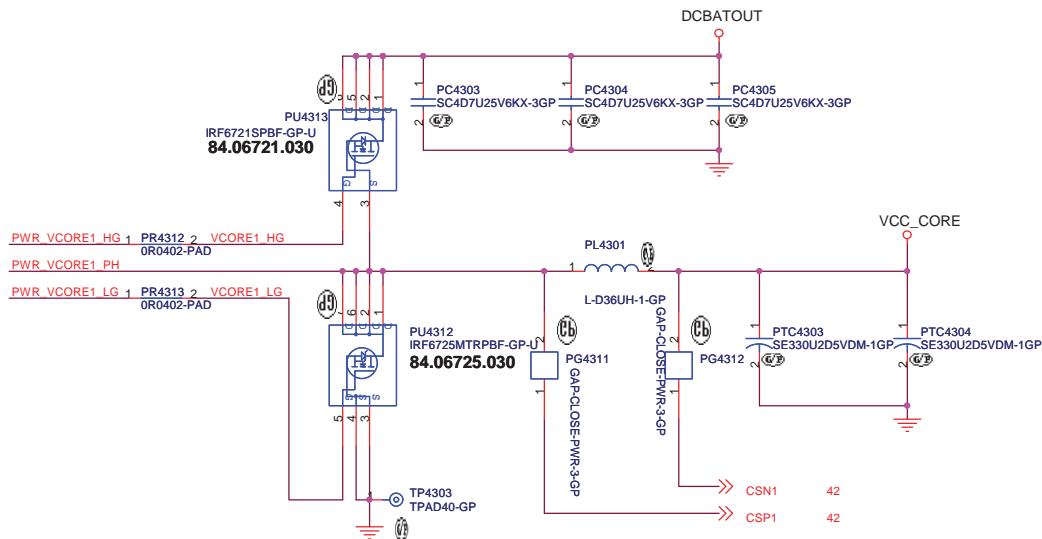
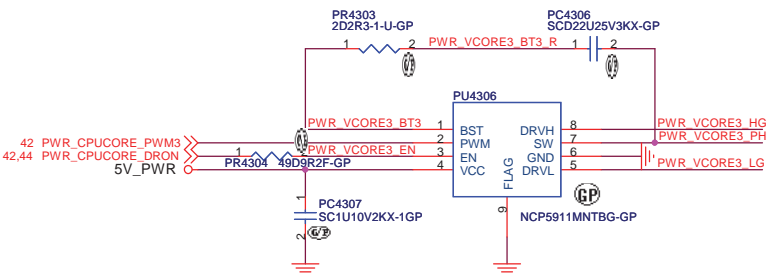
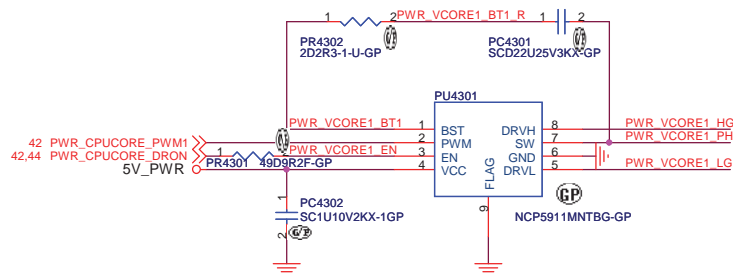
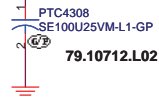
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
DC/DC 3D3V5V			
Size	Document Number		Rev
	LLW-1 / LGG-1		-1
Date:	Tuesday, January 18, 2011	Sheet 41 of 94	

DCBATOUT



DCBATOUT

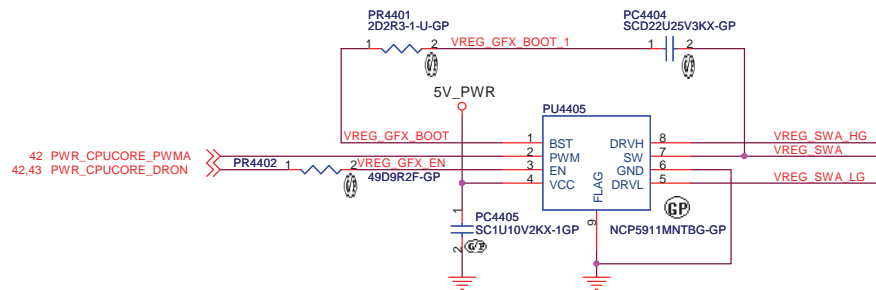
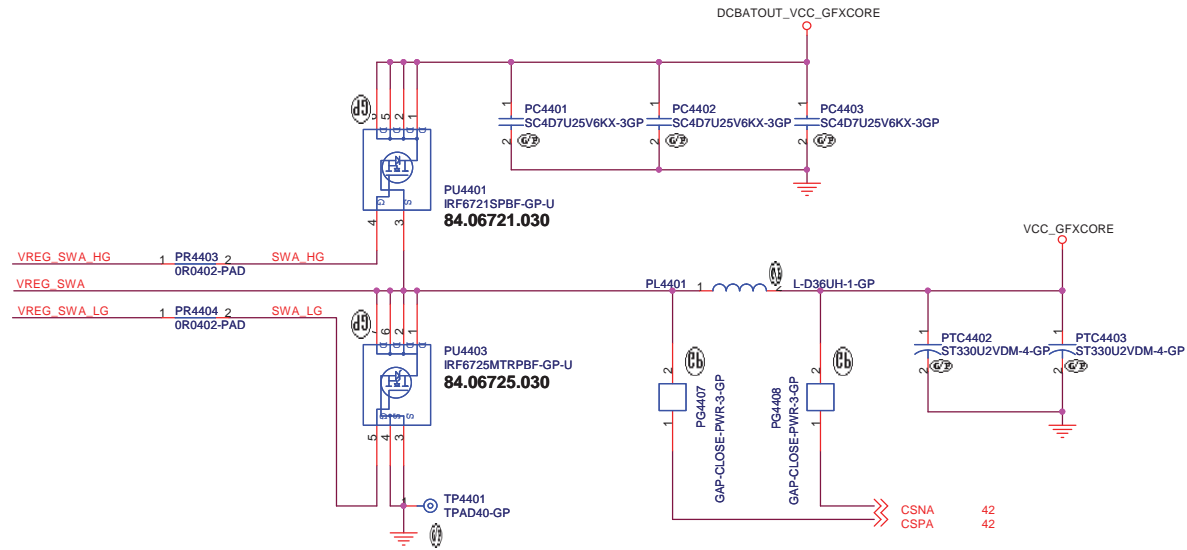
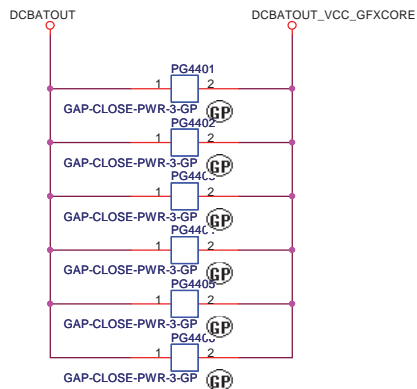


<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title DC/DC CPU CORE2_NCP6131
Size Document Number LLW-1 / LGG-1 Rev -1

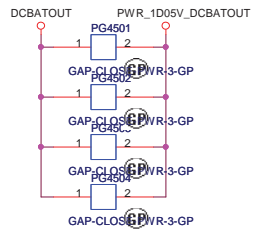
Date: Tuesday, January 18, 2011 Sheet 43 of 94



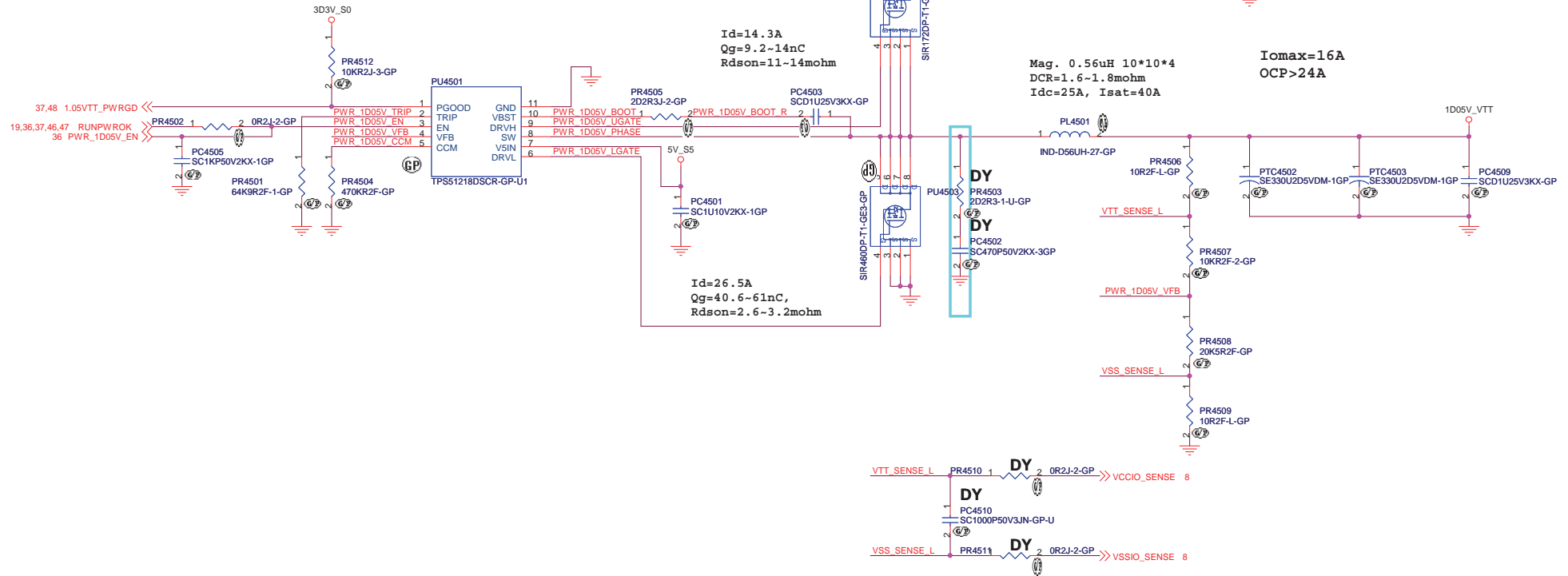
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			DC/DC CPU CORE3_NCP6131	
Size	Document Number	LLW-1 / LGG-1		Rev
				-1
Date:	Tuesday, January 18, 2011	Sheet	44	of 94



TPS51218 for 1D05V



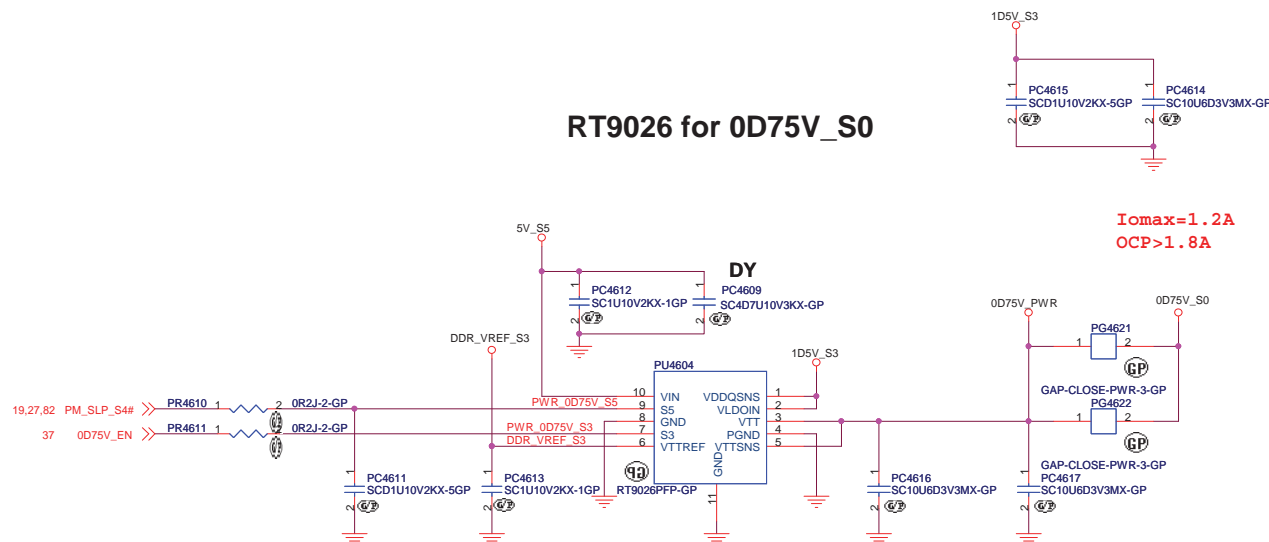
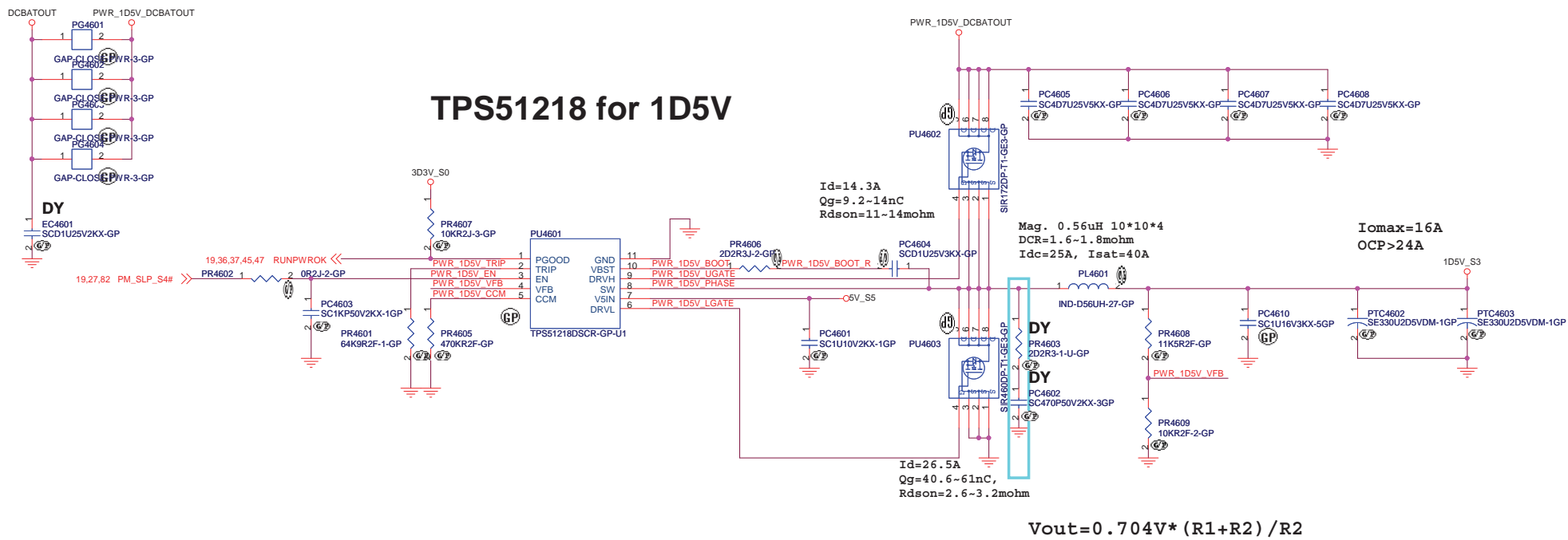
$$V_{out}=0.704V \cdot (R1+R2) / R2$$

<Core Design>

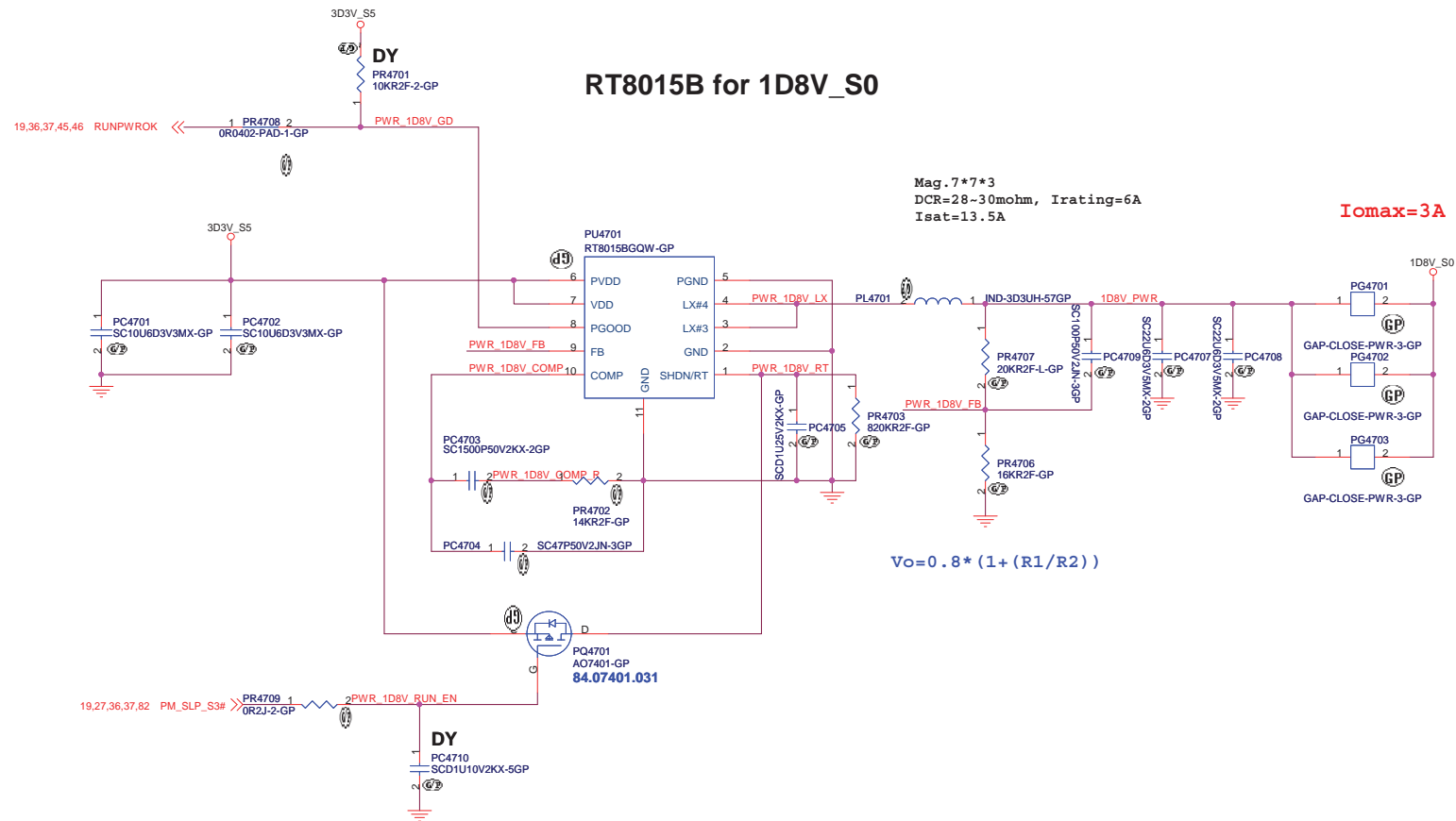
緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		TPS51218_1D05V	
Size	Document Number	LLW-1 / LGG-1	Rev
Date	Tuesday, January 18, 2011	Sheet 45	of 94



<Core Design>

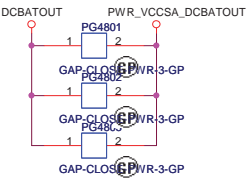


<Core Design>

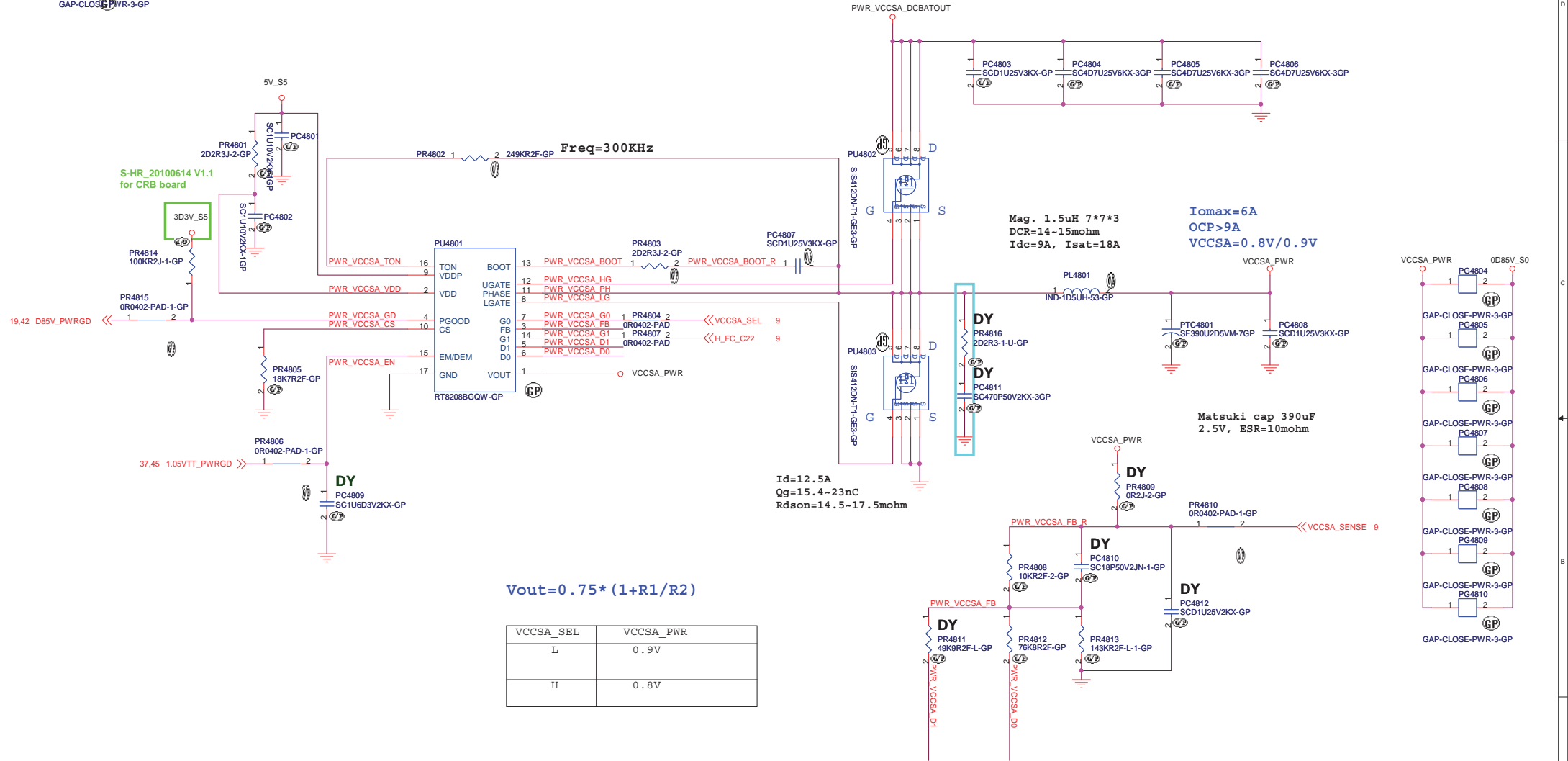
緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

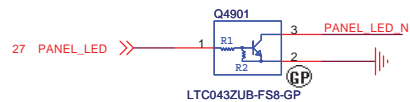
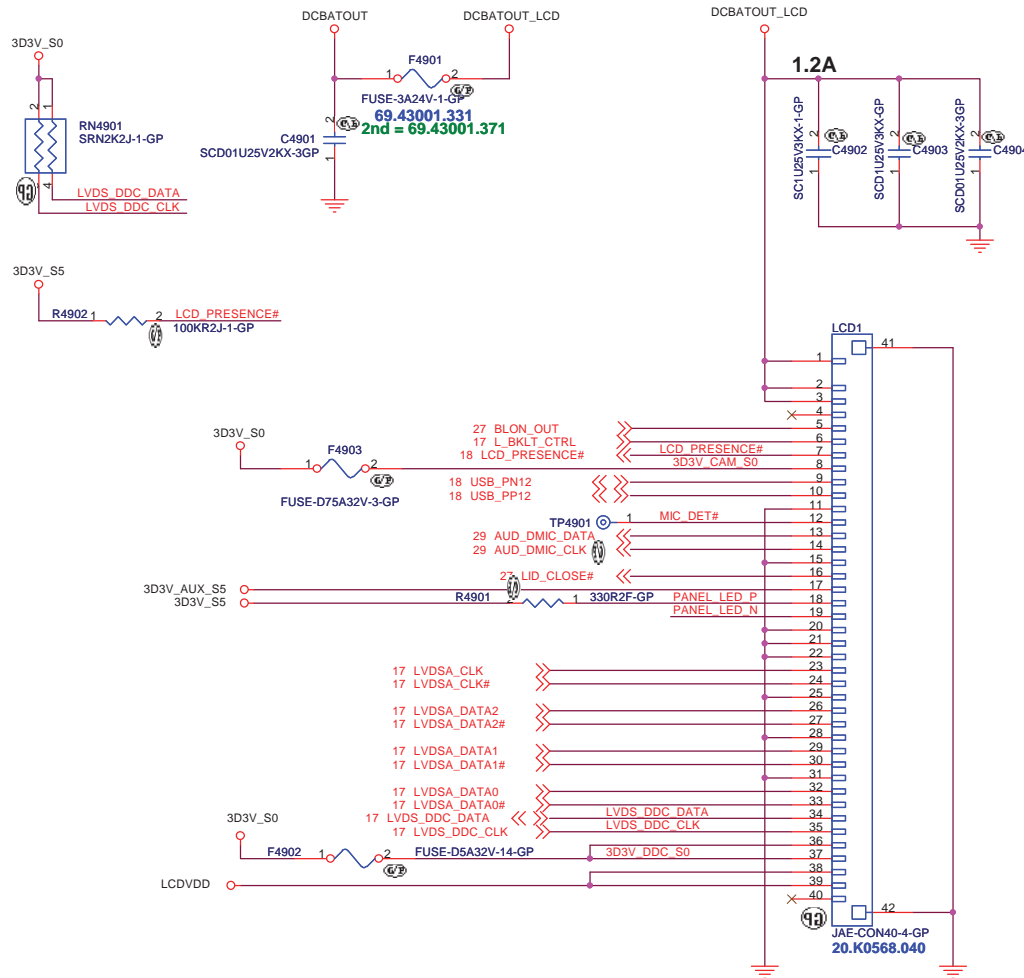
Title		PWM_1D8V_RT8015B	
Size	Document Number	LLW-1 / LGG-1	
Date	Tuesday, January 18, 2011	Sheet	47 of 94
		Rev	-1



RT8208A for VCCSA



LCD / Inverter Connector



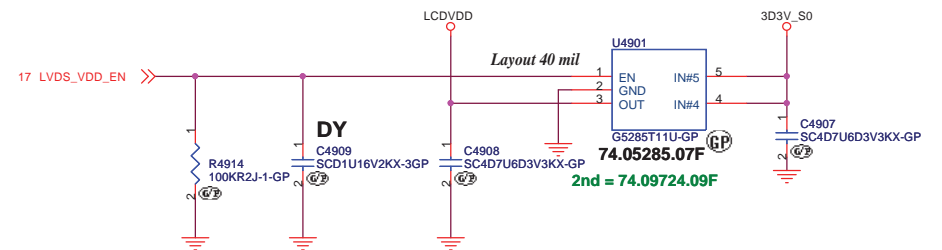
Near LCD1

LID_CLOSE# 1 AFTP4901 AFTE14P-GP

AUD_DMIC_CLK 1 AFTP4902 AFTE14P-GP

AUD_DMIC_DATA 1 AFTP4903 AFTE14P-GP

3D3V_DDC_S0 1 AFTP4904 AFTE14P-GP



<Core Design>

緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

LCD CONNECTOR

Size
A3

Document Number

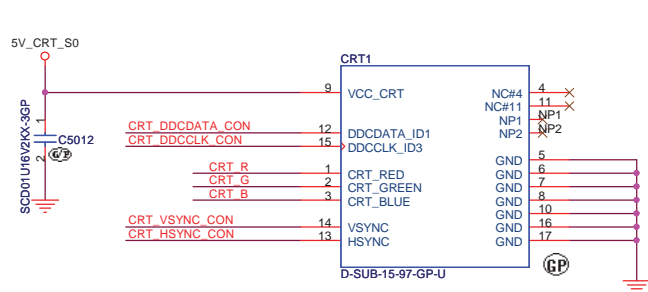
LLW-1 / LGG-1

Rev
-1

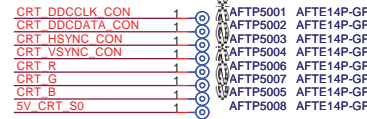
Date: Tuesday, January 18, 2011

Sheet 49 of 94

CRT CONNECTOR

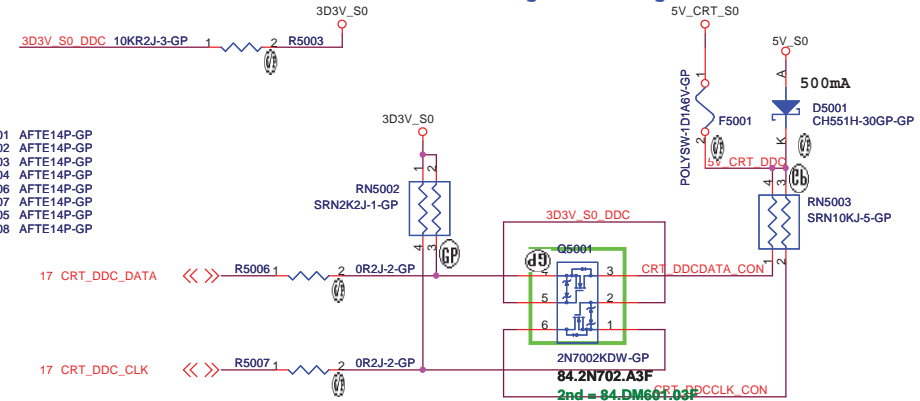


Near CRT1

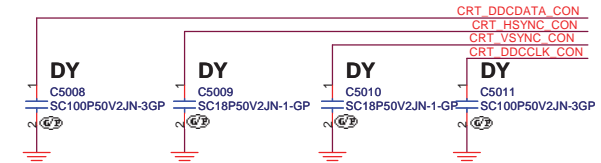
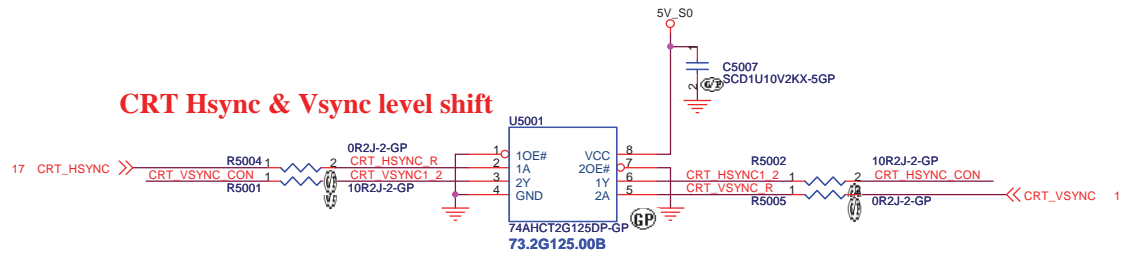


CRT DDCDATA & DDCCLK level shift

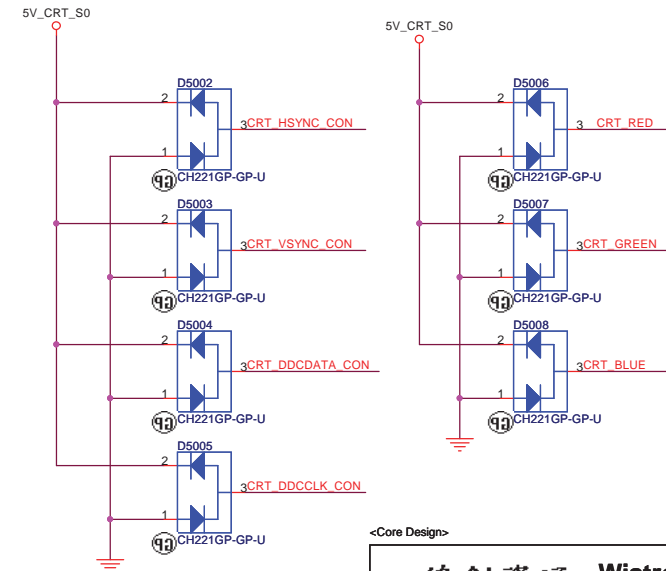
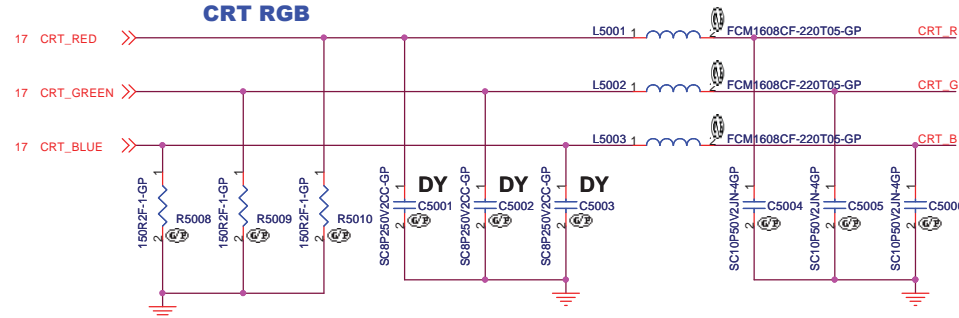
Pull High 5V Design on CRT Board



CRT Hsync & Vsync level shift



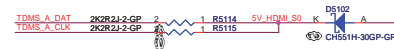
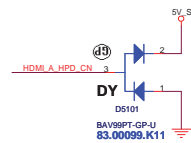
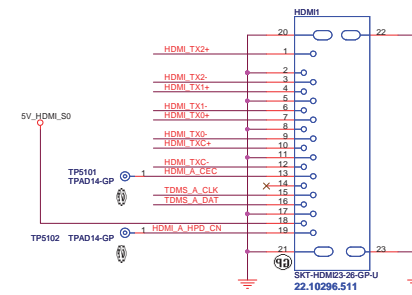
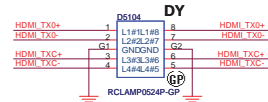
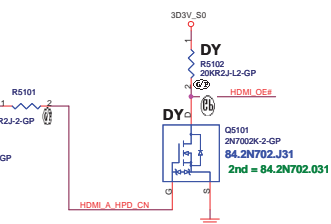
CRT RGB



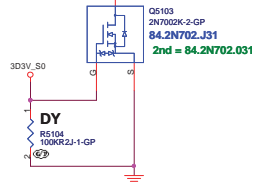
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			CRT Connector	
Size	Document Number	Rev		-1
A3	LLW-1 / LGG-1			
Date:	Tuesday, January 18, 2011	Sheet	50	of 94



Close to HDMI Connector



Pin configuration diagram for the 2N7002N GP MOSFET. The gate is connected to 303V_S0. The drain is connected to PCH_HDMI_DATA. The source is connected to PCH_HDMI_CLK. The MOSFET is labeled 2N7002N GP, 84.2N702.A3F, and 2nd = 84.DM601.03F.

BLANK

<Core Design>

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title <div>DISPLAY PORT CONNECTOR</div>		
Size <div>A4</div>	Document Number <div>LLW-1 / LGG-1</div>	Rev <div>-1</div>
Date: Tuesday, January 18, 2011		Sheet 52 of 94

D

C

B

A

BLANK

<Core Design>

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title <div>BLANK</div>		
Size <div>A4</div>	Document Number <div>LLW-1 / LGG-1</div>	Rev <div>-1</div>
Date: Tuesday, January 18, 2011		
Sheet 53 of 94		

D

C

B

A

BLANK

<Core Design>

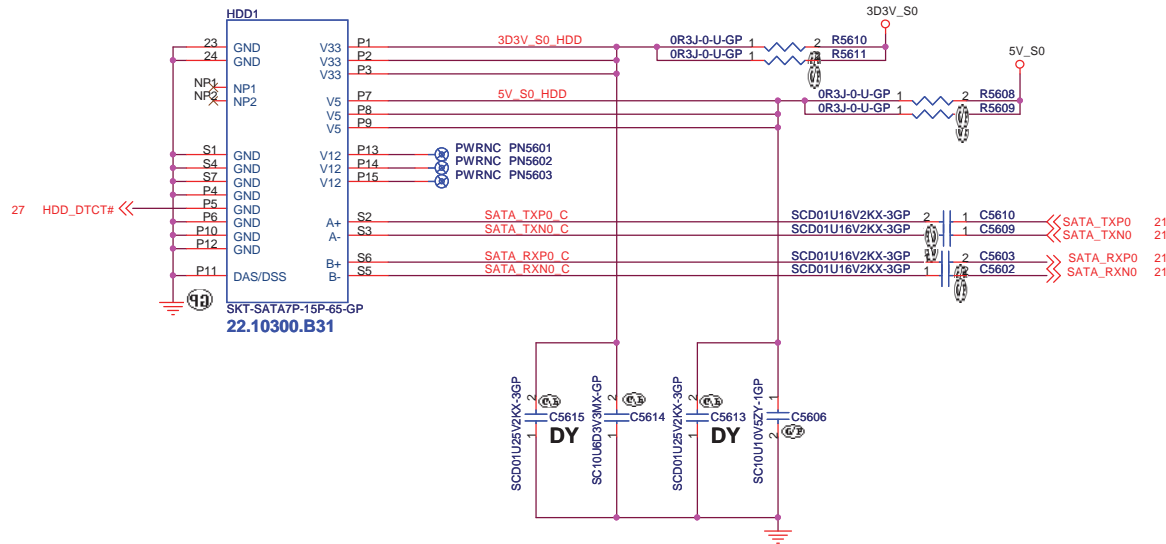
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>BLANK</div>		
Size <div>A4</div>	Document Number <div>LLW-1 / LGG-1</div>	Rev <div>-1</div>
Date: Tuesday, January 18, 2011		
Sheet 54 of 94		

	A	B	C	D	E
4					
3					
2					
1					
	A	B	C	D	E

<Core Design>

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title		
FAN CONTROL		
Size	Document Number	Rev
A4	LLW-1 / LGG-1	-1
Date:	Tuesday, January 18, 2011	Sheet 55 of 94

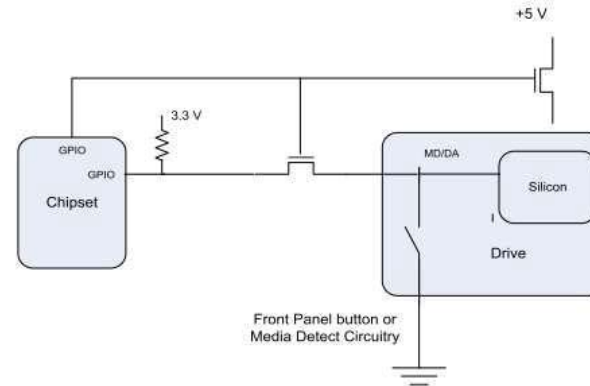
HDD Connector



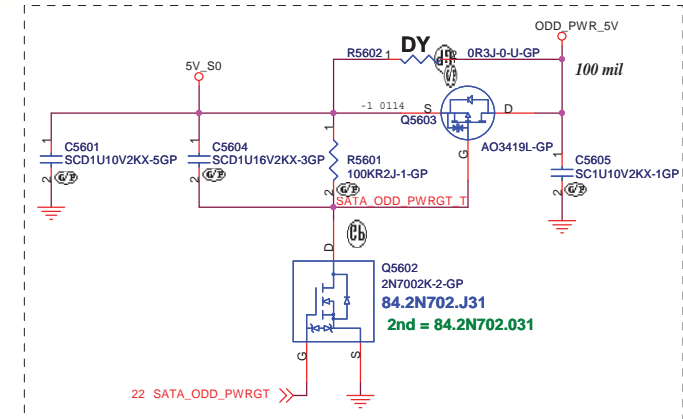
ODD Connector

SATA_RX- and SATA_RX+ Trace
Length match within 20 mil

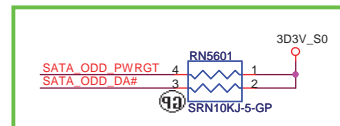
Mars:
Exchange ODD and ESATA differential pair each other.



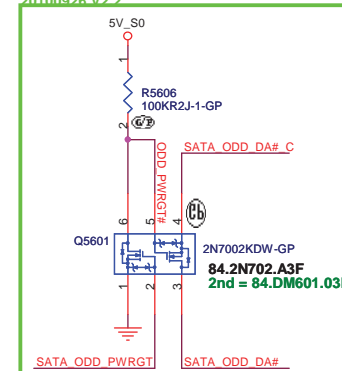
SATA Zero Power ODD



When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON

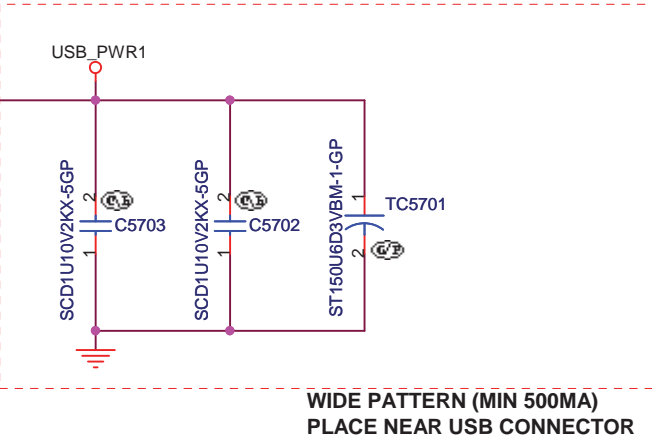
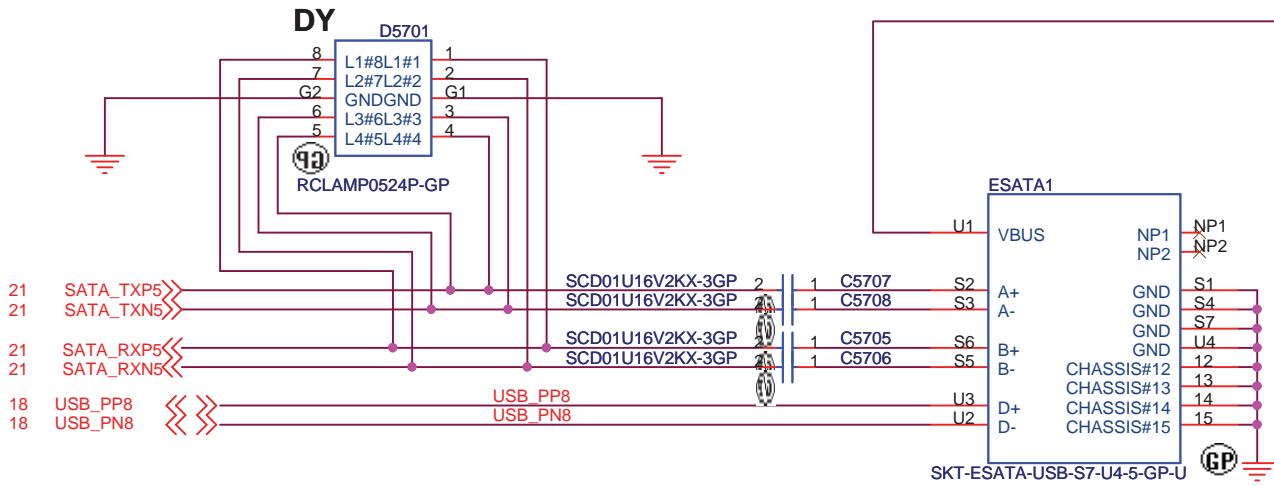


SUPPORT ZERO SATA ODD



0707 Modify:
Change Q5601 to DUAL 2N7002 for isolate MD/DA signal between PCH and ODD.

ESATA Connector



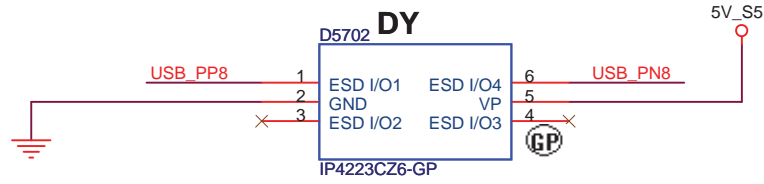
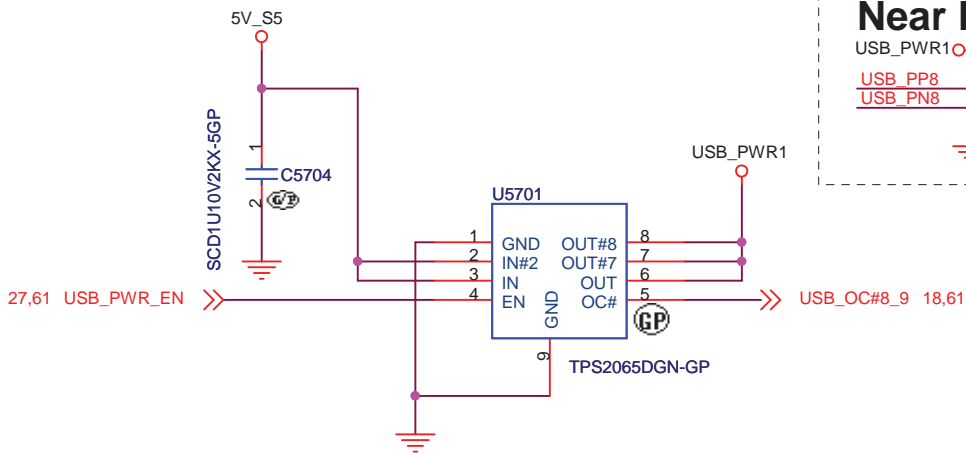
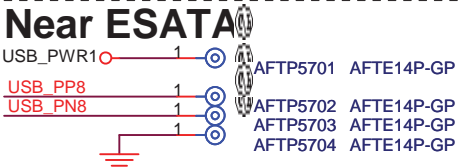
WIDE PATTERN (MIN 500MA)
PLACE NEAR USB CONNECTOR

Table 57.1- USB2.0 PWR SW multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
TI	TPS2065DGN4	54Y9024BA	74.02065.079
ROHM	BD8012FVJ	54Y9024AA	74.08012.07G

Table 57.2- 150U 6.3V POSCAP multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
NEC-TOKIN	TEPSLB20J157M	N/A	77.C1571.09L
SANYO	6TPE150MAZB	N/A	77.21571.111
HPC	TNCB0J157MTRZTF	N/A	80.15715.12L



<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

ESATA CONNECTOR

Size A4

Document Number

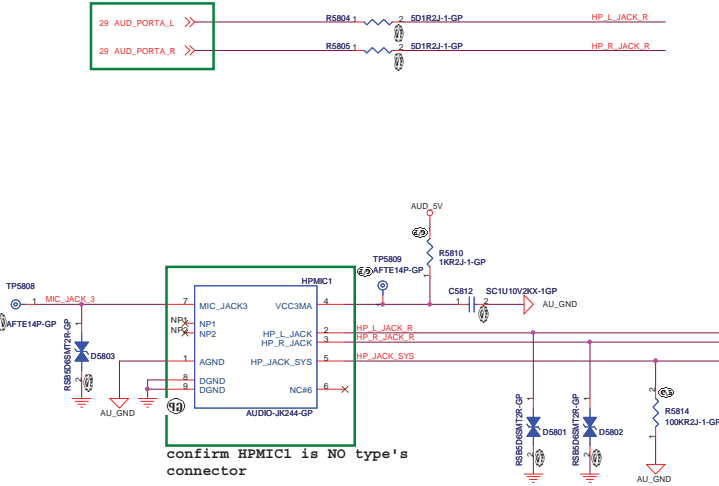
LLW-1 / LGG-1

Rev -1

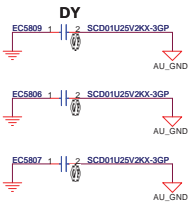
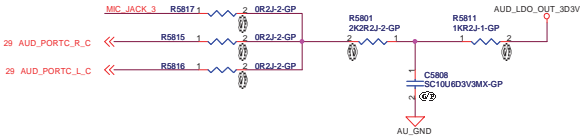
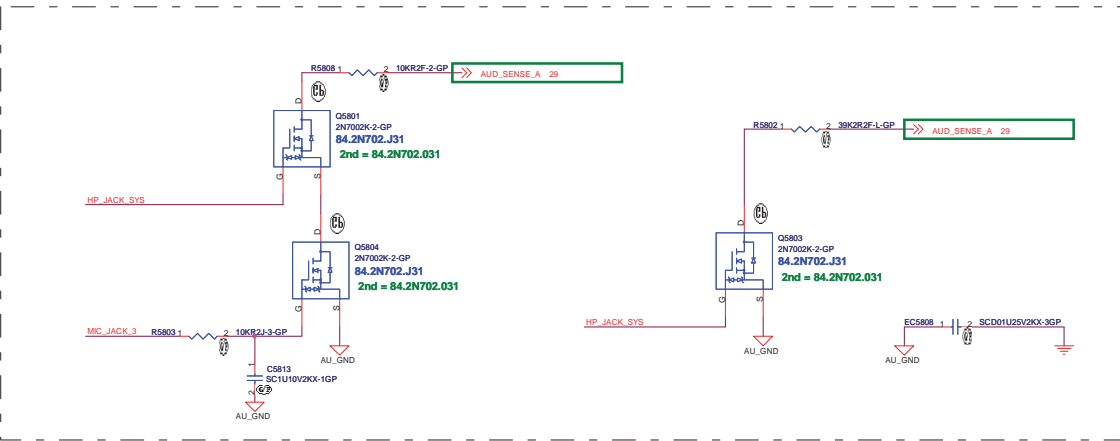
Date: Tuesday, January 18, 2011

Sheet 57 of 94

NEAR HEADPHONE CONN



JACK SENSE



INTERNAL STEREO SPEAKERS

Port G

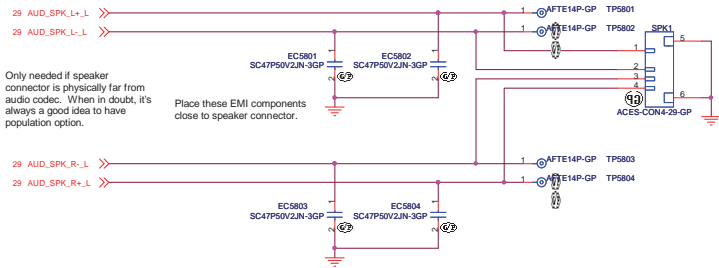
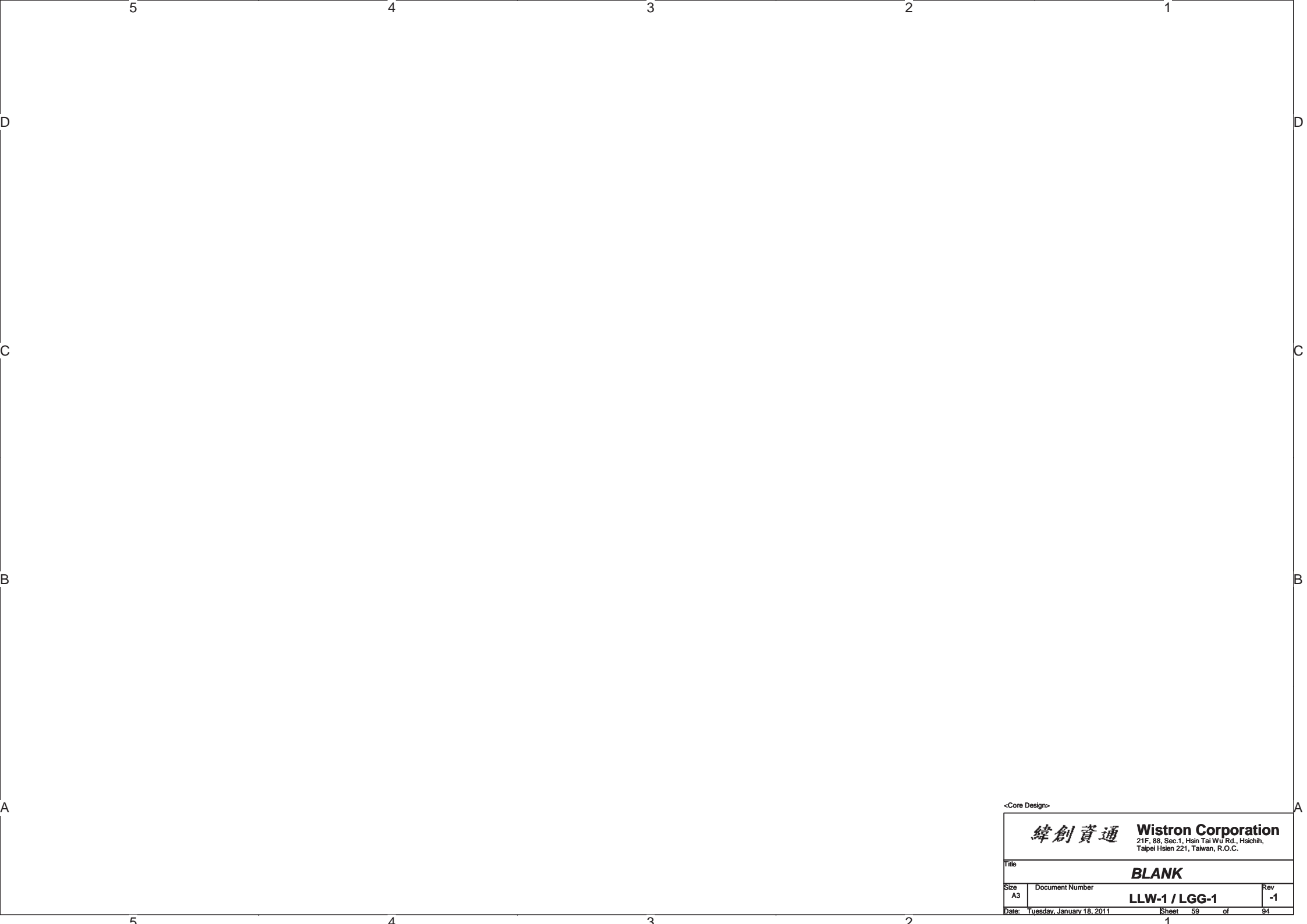


Table 58.1 - Bi-direction ESD multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ROHM	RSB5.6SMT2R	N/A	83.RSB56.BAF
ON SEMI	ESD5B5.0ST1G	N/A	83.ESD5B.0AF
NXP	PESD5V0S1BB	N/A	83.0005V.0AF

<Core Design>

緯創資通		Wistron Corporation	
21F, 8th, Sec.1, Hsin Tai Wu Rd., Hsichia, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
Audio Jack			
Size	Document Number	Rev	
A2	LLW-1 / LGG-1	-1	
Date: Tuesday, January 16, 2011		Sheet	66 of 94



<Core Design>		
<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title		
BLANK		
Size	Document Number	Rev
A3	LLW-1 / LGG-1	-1
Date: Tuesday, January 18, 2011	Sheet 59 of 94	1

```
SSID = Flash.ROM
```

SPI FLASH ROM (4M byte) for PCH

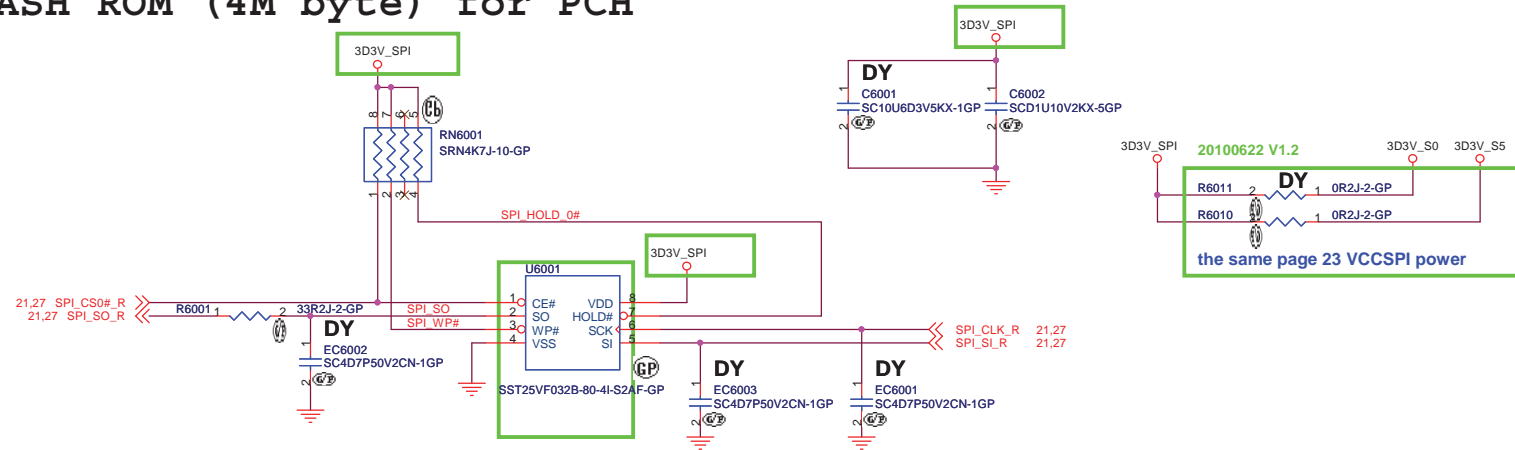


Table 60.1- SPI Serial Flash Memory multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
MXIC	MX25L3206EM2I-12G	N/A	72.25320.C01
WINBOND	W25Q32BVSSIG	N/A	72.25Q32.A01
NUMONYX	M25PX32-VMW6F	N/A	72.25P32.C01

SSID = RBATT

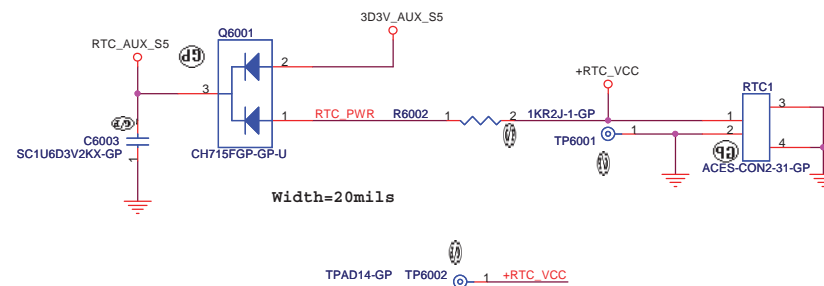


Table 60.2 - Schottky Barrier Diode multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
CHENMKO	CH715FGP	N/A	83.R0304.D81
CHENMKO	BAS40CWGP	N/A	83.00040.R81
PANJIT	BAS40CW	N/A	83.00040.E81

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Flash/RTC

Size
A3

Document Number

LLW-1 / LGG-1

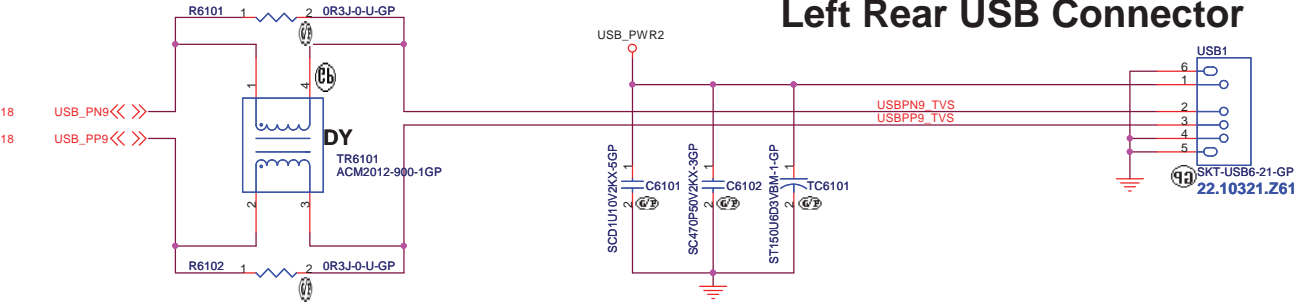
Date: Tuesday, January 18, 2011

Sheet 60 of 94

-1

USB Connector

WIDE PATTERN (MIN 500MA)
PLACE NEAR USB CONNECTOR



WIDE PATTERN (MIN 500MA)
PLACE NEAR USB CONNECTOR

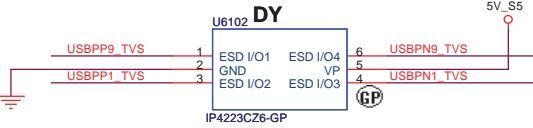
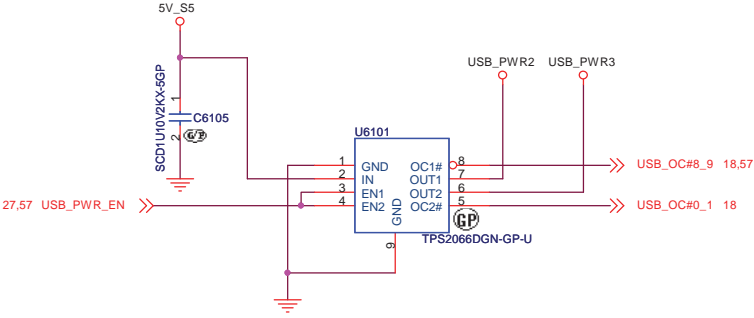
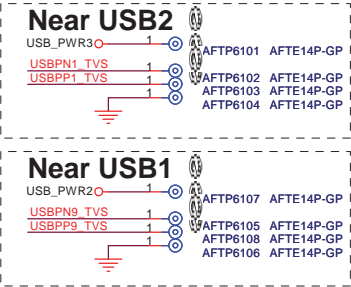
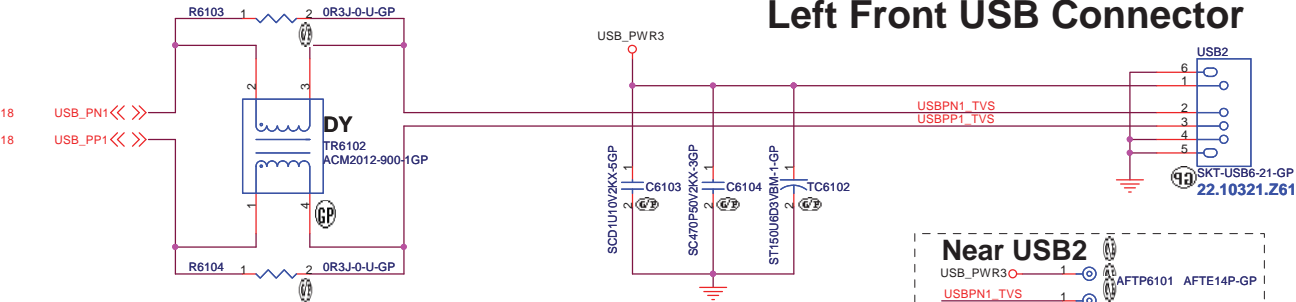


Table 61.1- USB2.0 PWR SW multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
TI	TPS2066DGN	41R0511AA	74.02066.A71
TI	TPS2066DGN-1	N/A	74.02066.B71

Table 61.2- 150U 6.3V POSCAP multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
NEC-TOKIN	TEPSLB20J157M	N/A	77.C1571.09L
SANYO	6TPE150MAZB	N/A	77.21571.111
HPC	TNCB0J157MTRZTF	N/A	80.15715.12L

<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

USB Connector

Size A3

Document Number

LLW-1 / LGG-1

Rev

-1

Date: Tuesday, January 18, 2011

Sheet 61 of 94

5

4

3

2

1

D

C

B

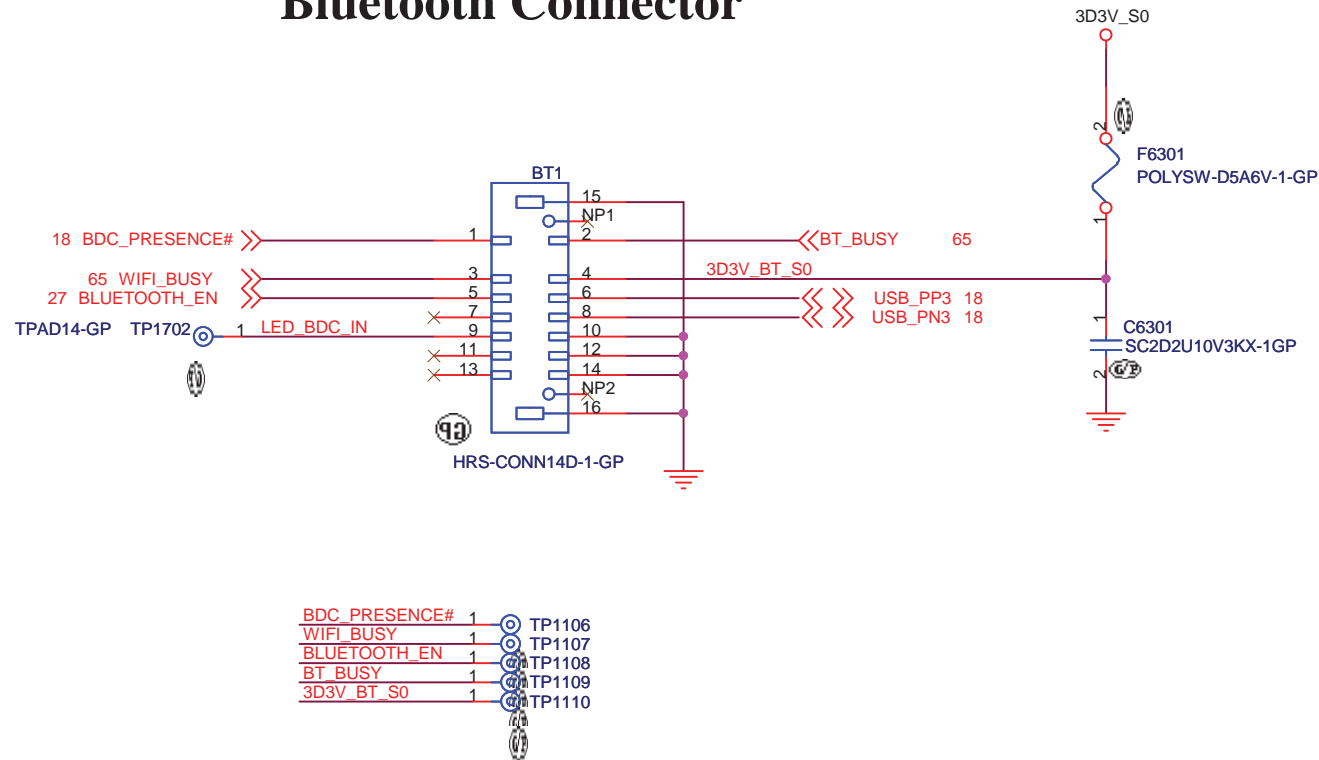
A

BLANK

<Core Design>

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title <div>BLANK</div>		
Size <div>A4</div>	Document Number <div>LLW-1 / LGG-1</div>	Rev <div>-1</div>
Date: Tuesday, January 18, 2011Sheet 62 of 94		

Bluetooth Connector



<Core Design>

緯創資通

Wistron Corporation21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

BluetoothSize
A4

Document Number

LLW-1 / LGG-1Rev
-1

Date: Tuesday, January 18, 2011

Sheet 63 of 94

D

C

B

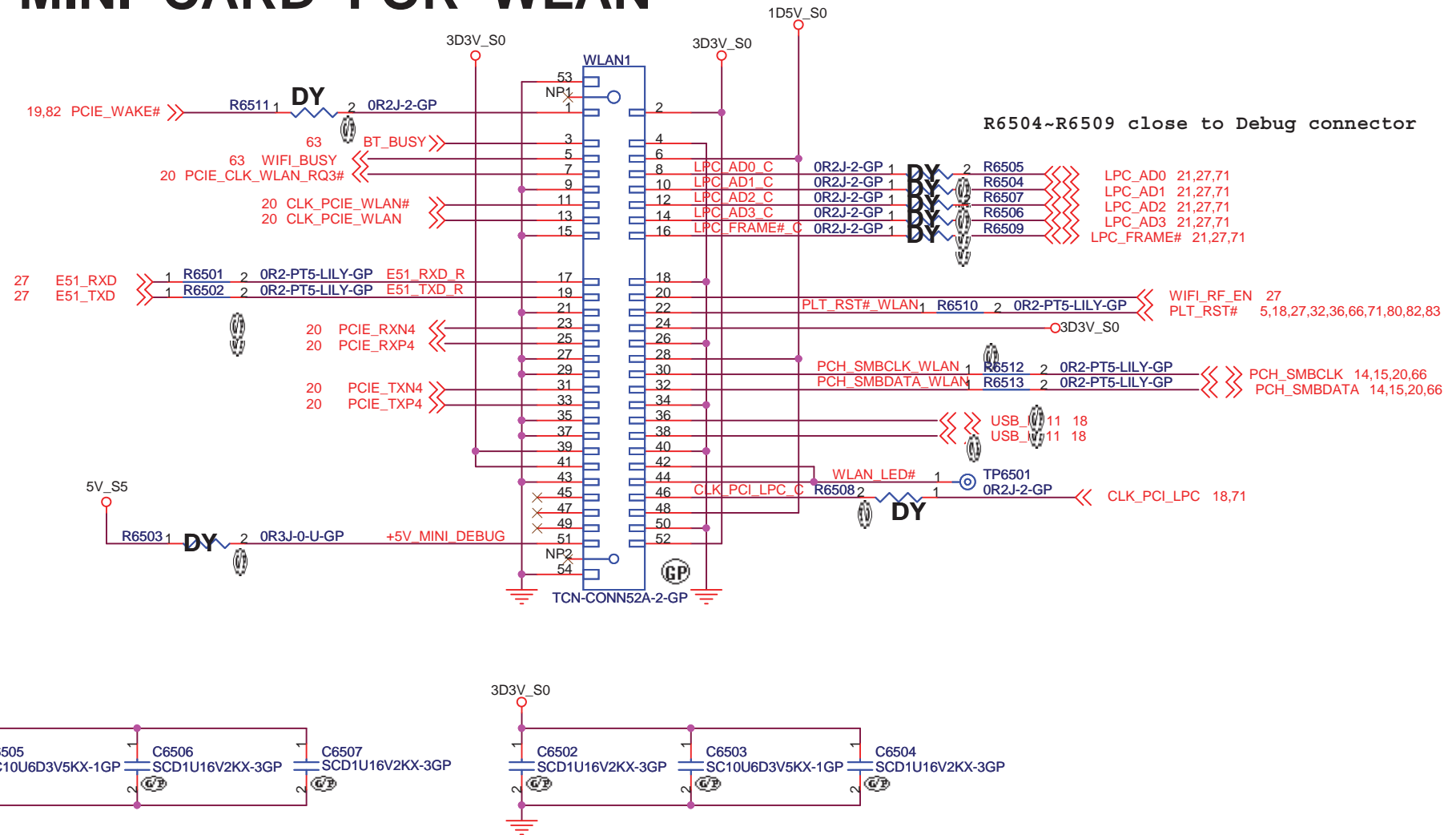
A

BLANK

<Core Design>

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>FingerPrint</div>		
Size <div>A4</div>	Document Number <div>LLW-1 / LGG-1</div>	Rev <div>-1</div>
Date: Tuesday, January 18, 2011		
Sheet 64 of 94		

HALF MINI CARD FOR WLAN



<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

MINI CARD SLOT 1

Size
A4

Document Number

LLW-1 / LGG-1

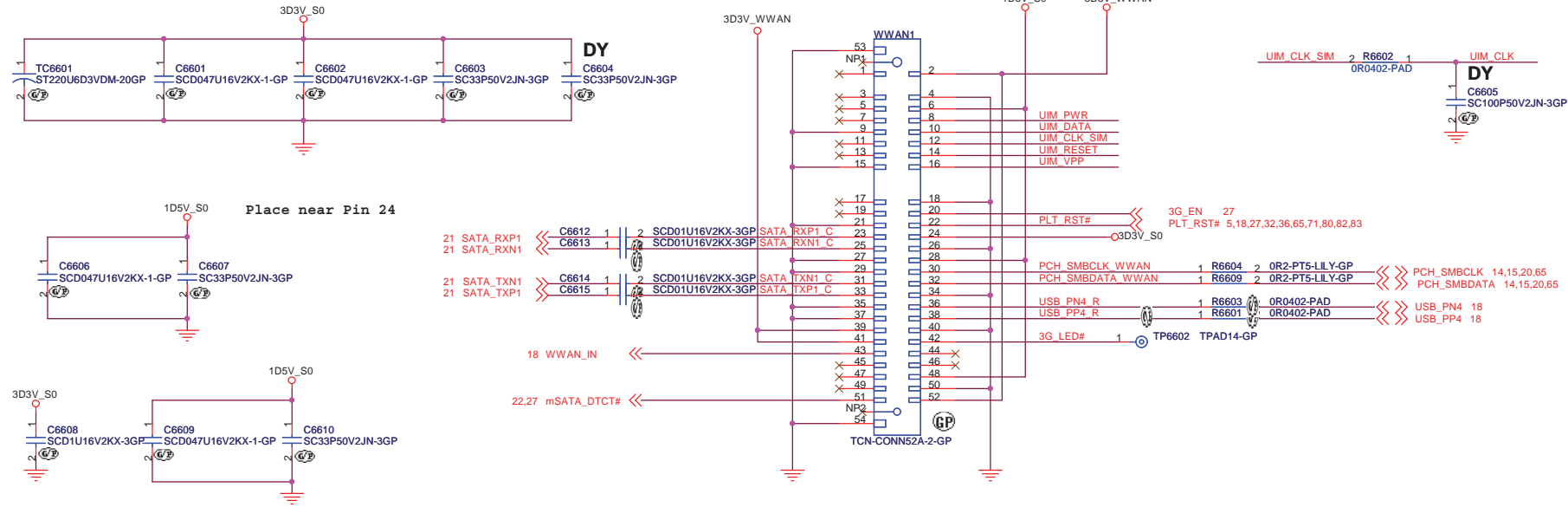
Rev
-1

Date: Tuesday, January 18, 2011

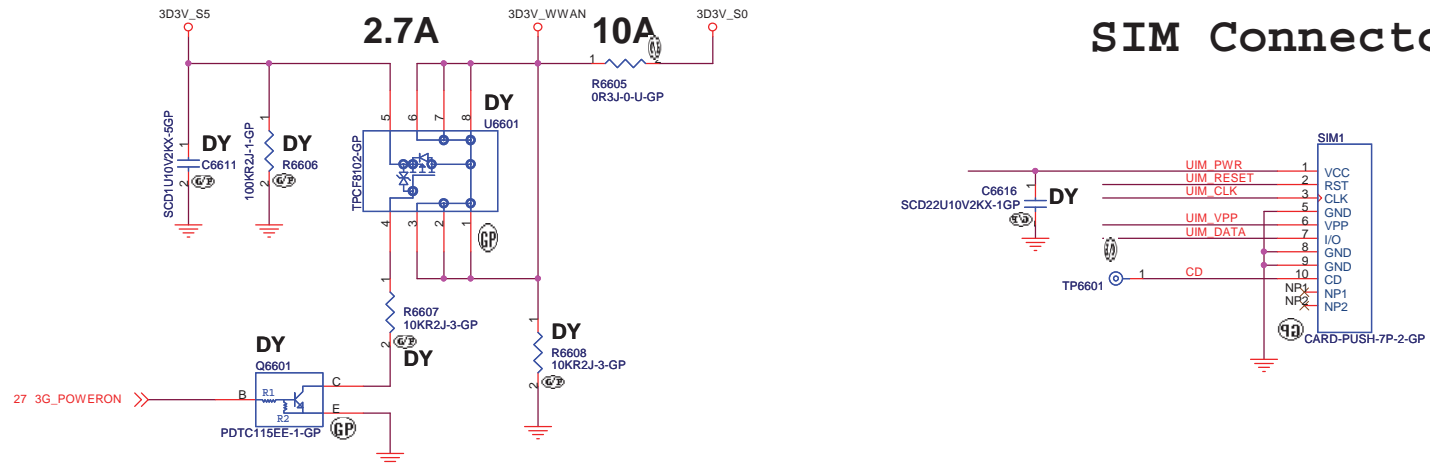
Sheet 65 of 94

Mini Card Connector(WWAN)

Place near MINI Card CONN



SIM Connector



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
MINI CARD SLOT 2		
Size	Document Number	Rev
A3	LLW-1 / LGG-1	-1
Date:	Tuesday, January 18, 2011	Sheet 66 of 94

D

C

B

A

BLANK

<Core Design>

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title <div>BLANK</div>		
Size <div>A4</div>	Document Number <div>LLW-1 / LGG-1</div>	Rev <div>-1</div>
Date: Tuesday, January 18, 2011		
Sheet 67 of 94		

D

C

B

A

BLANK

<Core Design>

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title <div>BLANK</div>		
Size <div>A4</div>	Document Number <div>LLW-1 / LGG-1</div>	Rev <div>-1</div>
Date: Tuesday, January 18, 2011Sheet 68 of 94		

Touch Pad Connector

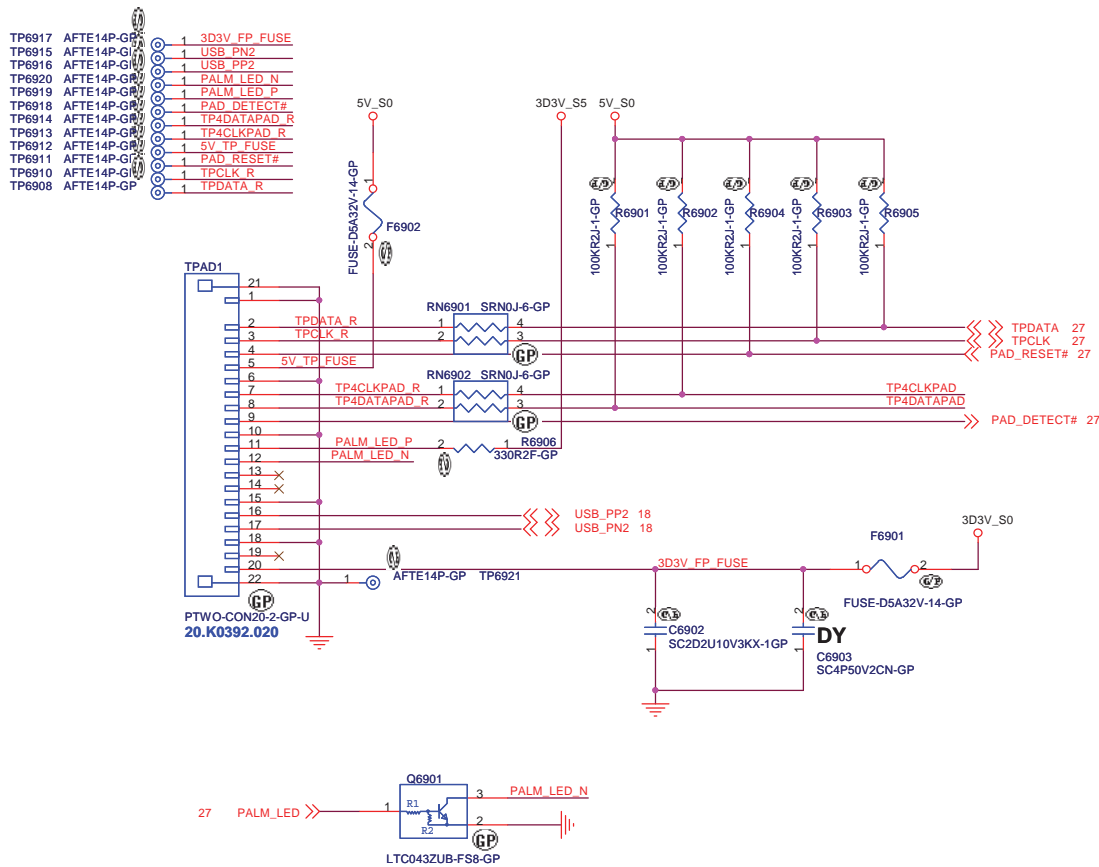
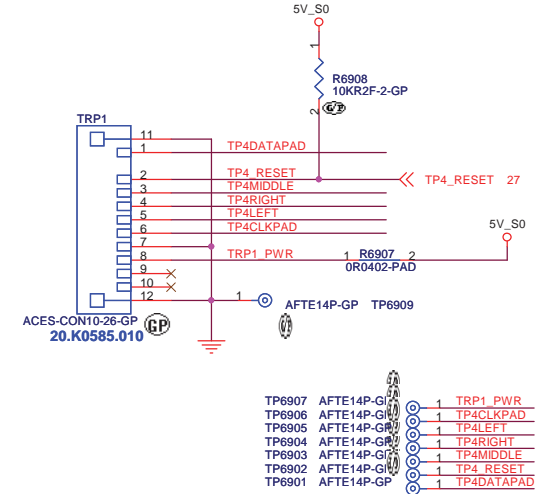


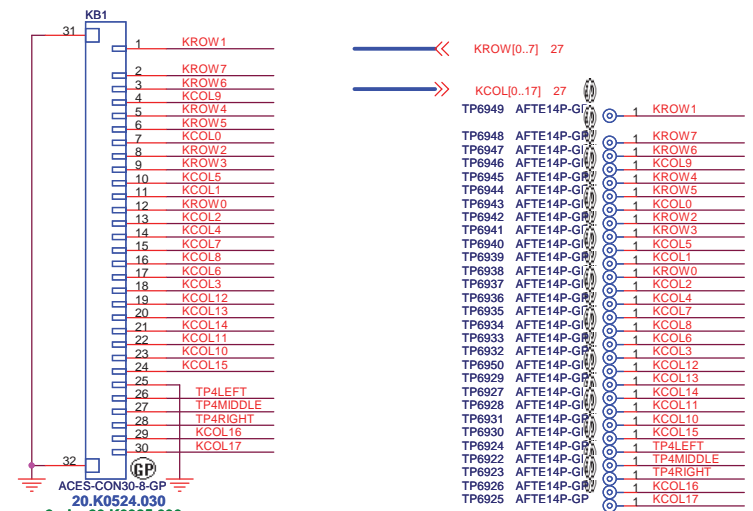
Table 69.1- Transistor multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
NXP	PDTC143ZU	N/A	84.00143.E1K
ROHM	LTC043ZUB	N/A	84.00043.011
Panasonic	DRC5143Z0L	N/A	84.05143.011

Track Point Connector



KeyBoard Connector



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
TOUCH PAD CONNECTOR			
Size A3	Document Number	LLW-1 / LGG-1	Rev -1
Date:	Tuesday, January 18, 2011	Sheet 69 of	94

D

C

B

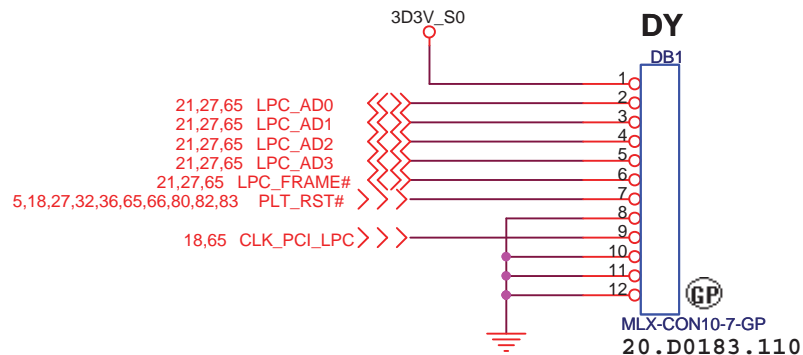
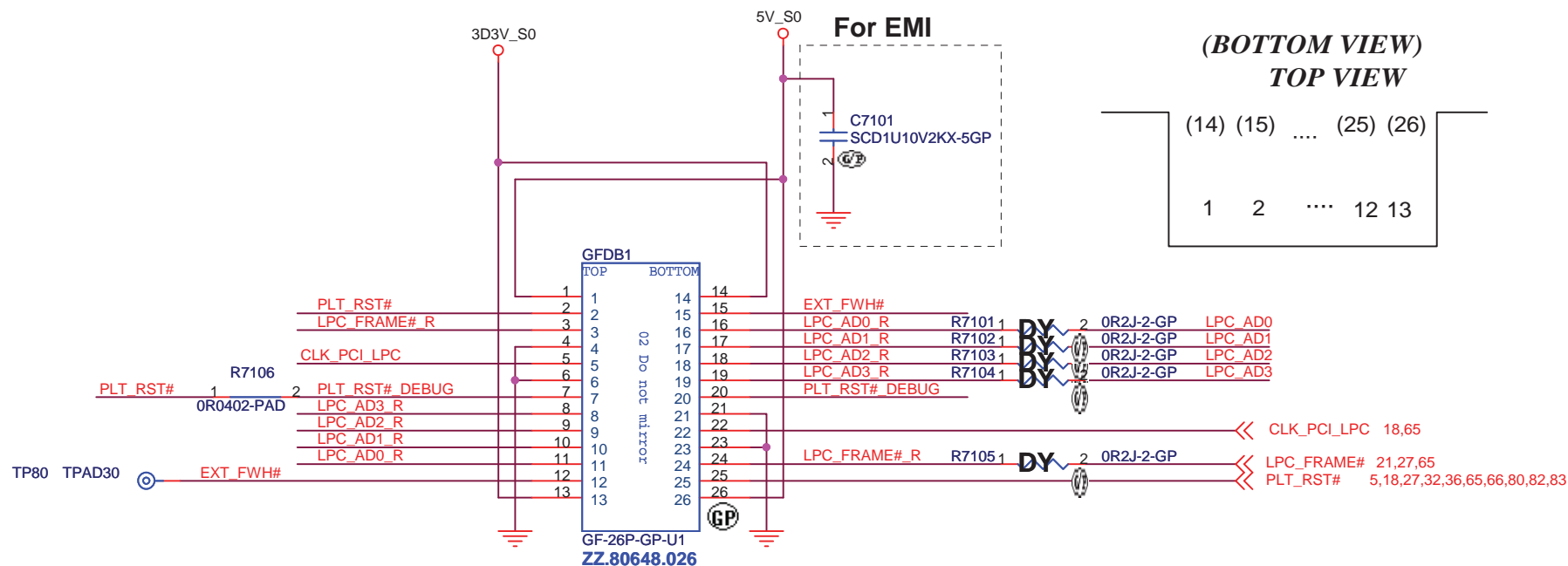
A

BLANK

<Core Design>

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title <div>BLANK</div>		
Size <div>A4</div>	Document Number <div>LLW-1 / LGG-1</div>	Rev <div>-1</div>
Date: Tuesday, January 18, 2011Sheet 70 of 94		

Golden Finger for Debug Board



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **DEBUG CONN**

Size A4 Document Number **LLW-1 / LGG-1** Rev -1

Date: Tuesday, January 18, 2011 Sheet 71 of 94

5

4

3

2

1

D

C

B

A

BLANK

<Core Design>

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title <div>BLANK</div>		
Size <div>A4</div>	Document Number <div>LLW-1 / LGG-1</div>	Rev <div>-1</div>
Date: Tuesday, January 18, 2011		
Sheet 72 of 94		

D

C

B

A

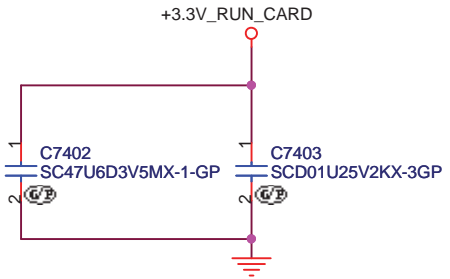
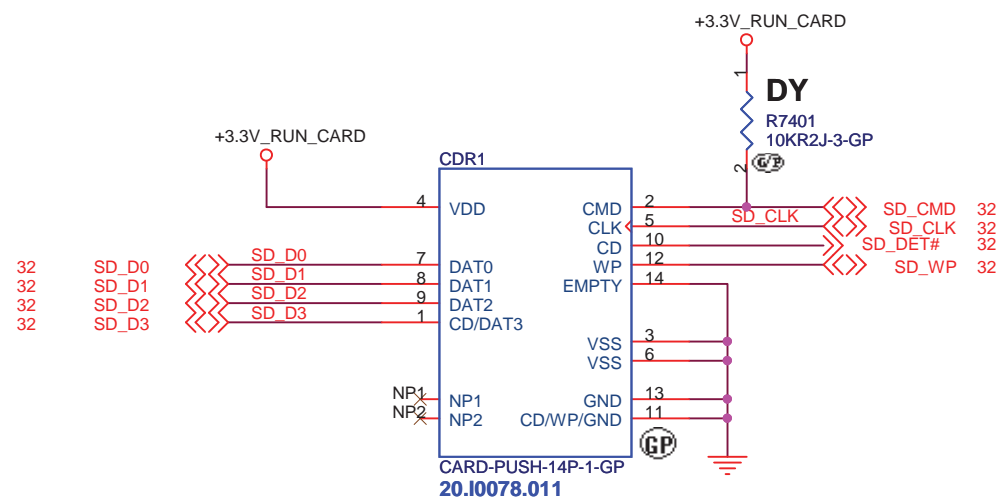
BLANK

<Core Design>

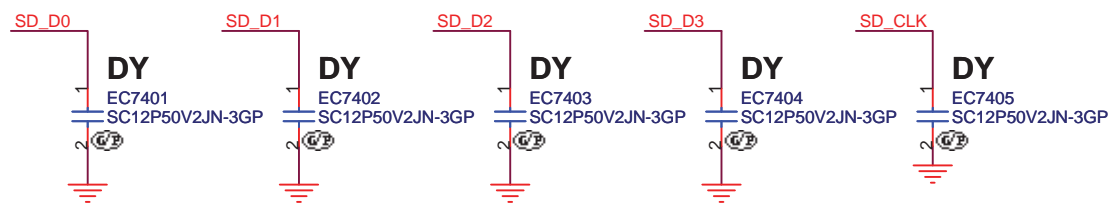
<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title <div>BLANK</div>		
Size <div>A4</div>	Document Number <div>LLW-1 / LGG-1</div>	Rev <div>-1</div>
Date: Tuesday, January 18, 2011		
Sheet 73 of 94		

Please apply Shield GND for SD_CLK signal between
R5U220 and SD Card Slot to decrease external noise.

Card Reader Connector



+3.3V_RUN_CARD trace = 40mil
C7402 lose CDR1



<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CARD Reader CONN

Size

Document Number

Rev

A4

LLW-1 / LGG-1

-1

Date:

Tuesday, January 18, 2011

Sheet

74

of

94

SSID = ExpressCard

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

New Card

Size
A3

Document Number
LLW-1 / LGG-1

Rev
-1

Date: Tuesday, January 18, 2011Sheet 75 of 94

D

C

B

A

BLANK

<Core Design>

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title <div>BLANK</div>		
Size <div>A4</div>	Document Number <div>LLW-1 / LGG-1</div>	Rev <div>-1</div>
Date: Tuesday, January 18, 2011		
Sheet 76 of 94		

BLANK

<Core Design>

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
TPM			
Size	Document Number		Rev
Custom	LLW-1 / LGG-1		-1
Date:	Tuesday, January 18, 2011	Sheet 77 of	94

D

C

B

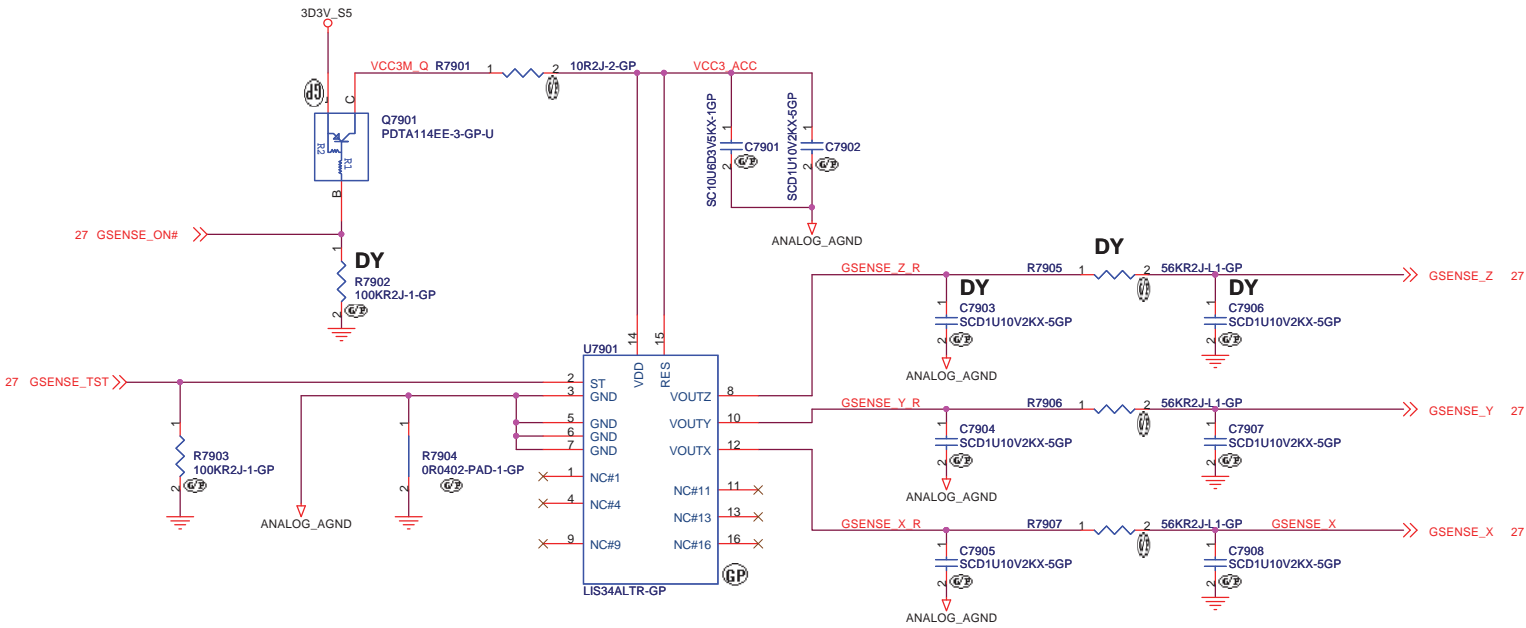
A

BLANK

<Core Design>

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title <div>BLANK</div>		
Size <div>A4</div>	Document Number <div>LLW-1 / LGG-1</div>	Rev <div>-1</div>
Date: Tuesday, January 18, 2011		
Sheet 78 of 94		

G-Sensor



	LIS34AL	No Accel
	KXTC8-2850	
R7902	NO_ASM	ASM
R7903	ASM	ASM
All other	ASM	NO_ASM

Layout Comment :

- (1) Place C7904, C7905, Q7901, R7901, R7902, C7901, C7902, R7903, R508 close to U7901.
- (2) Avoid routing under DCDC switching area.

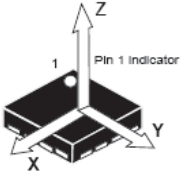


Table 79.1- Transistor multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
NXP	PDTA114EE	N/A	84.00114.H1K
ON	DTA114EET1G	N/A	84.DT114.B11
ROHM	LTA014EEB	N/A	84.00014.01H
Panasonic	DRA9114E0L	N/A	84.09114.A11

Table 79.2- Accelerometer multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ST	LIS34ALTR-GP	41R0828AA	74.00034.0BZ
ROHM-KIONIX	KXTC8-2850-GP	N/A	74.KXTC8.0BZ

<Core Design>

緯創資通 Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
G-Sensor		
Size	Document Number	Rev
Custom	LLW-1 / LGG-1	-1
Date:	Tuesday, January 18, 2011	Sheet 79 of 94

RFID

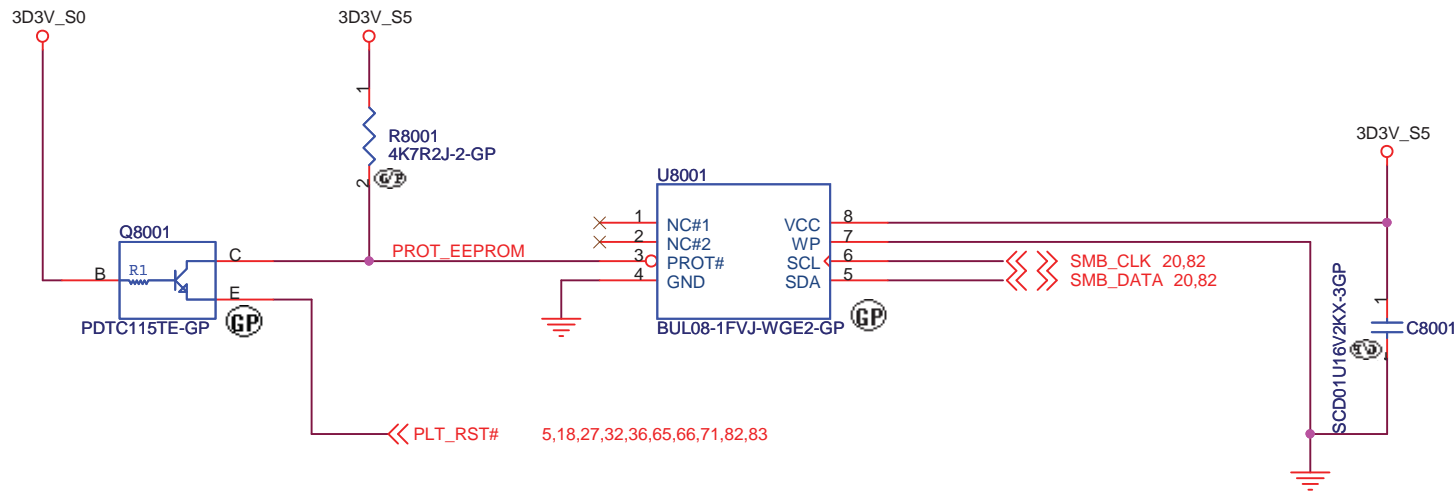



Table 80.1- Transistor multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
NXP	PDT115TE	N/A	84.00115.E1K
ROHM	LTC015EEB	N/A	84.00015.01H
Panasonic	DRC9115T0L	N/A	84.09115.A11

Table 80.2- EEPROM multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ROHM	BUL08-1FVJ-WGE2	N/A	72.BUL08.A0Q
NXP	PCA24S08ADP	N/A	72.24S08.A0Q
SANYO	LE26CAP08TT-TLM-H	N/A	72.26C08.00R

<Core Design>

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
RFID	
Size A4	Document Number LLW-1 / LGG-1
Date: Tuesday, January 18, 2011	Rev -1
Sheet 80 of 94	

BLANK

<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size

A3

Document Number

LLW-1 / LGG-1

Rev

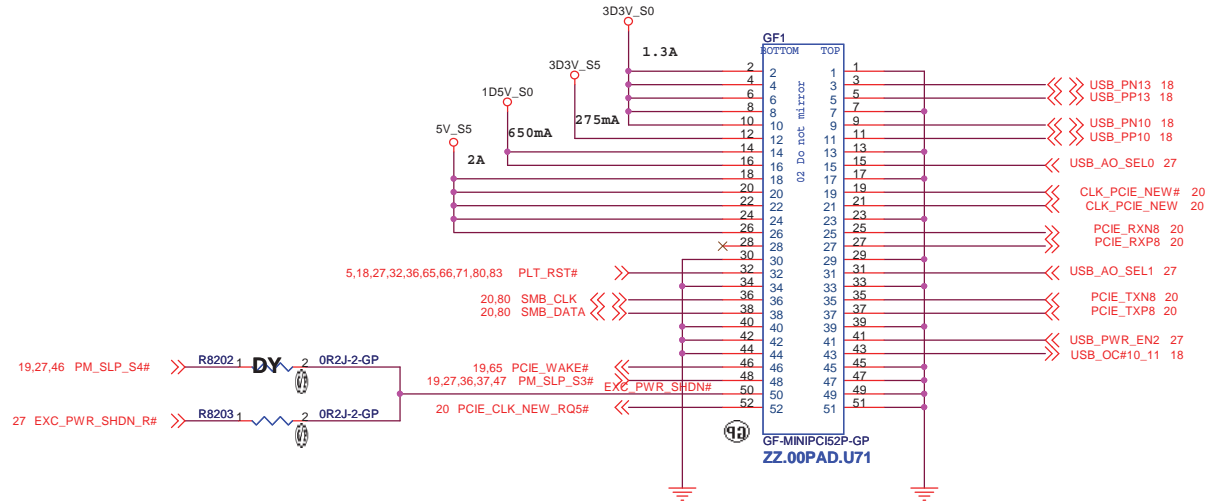
-1

Date: Tuesday, January 18, 2011

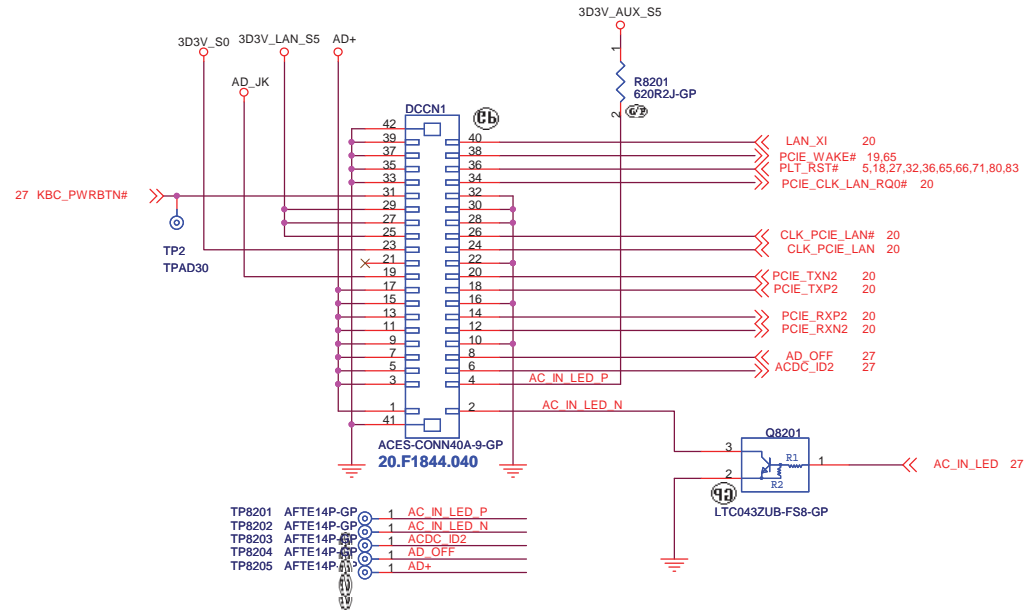
Sheet 81 of 94

1

TO EXP BOARD CONN



DC BOARD CONN



<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

IO Board Connector

Size

Document Number

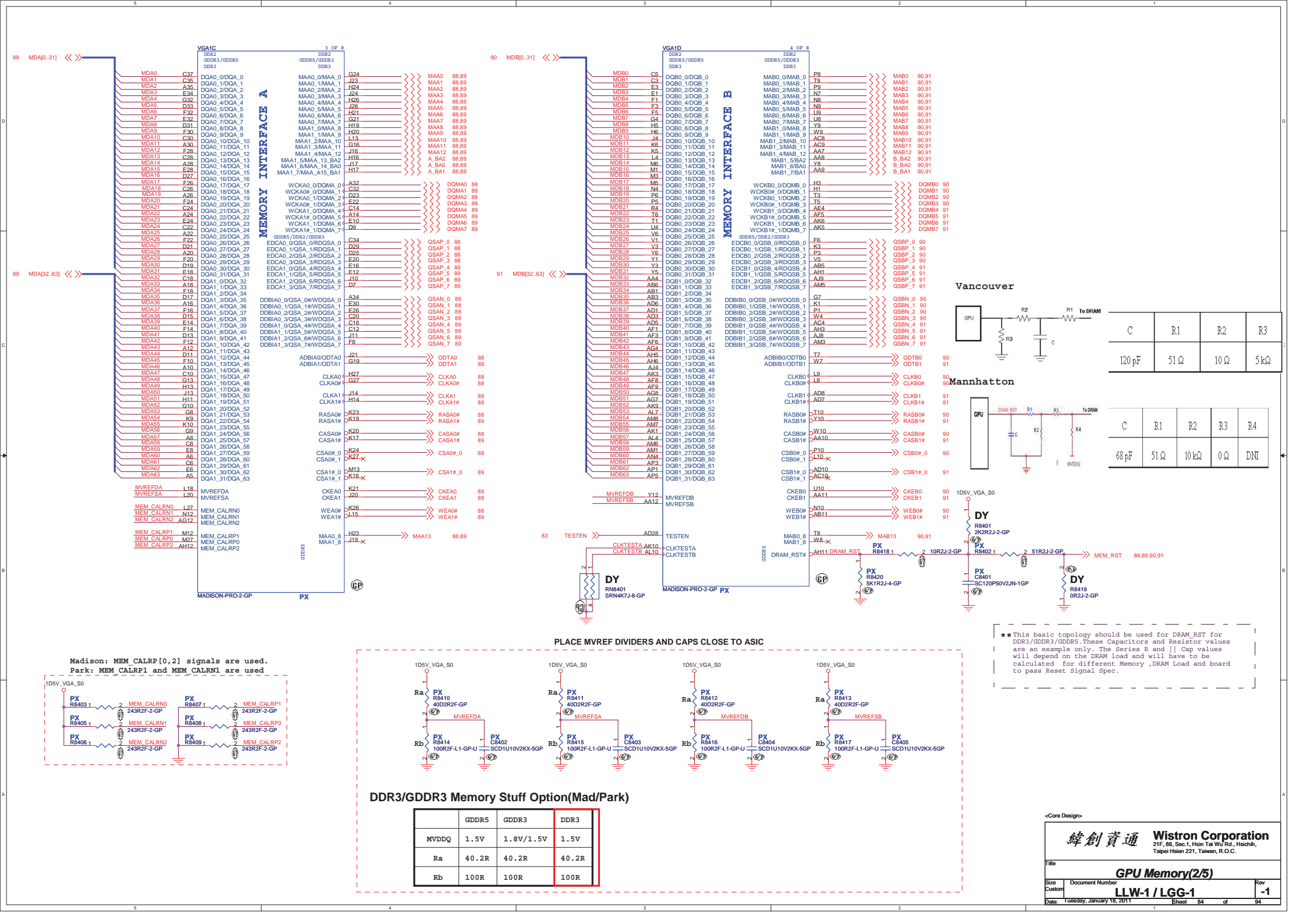
LLW-1 / LGG-1

ev

Date: Tuesday, January 18, 2011

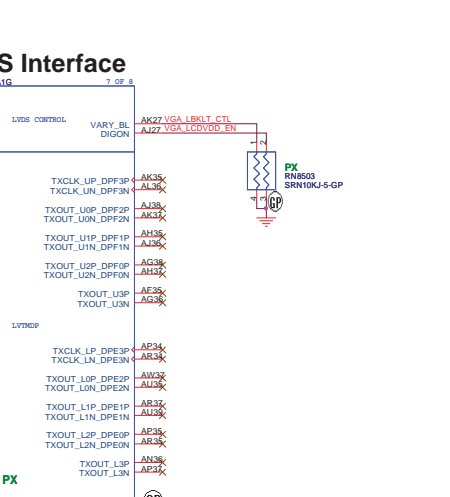
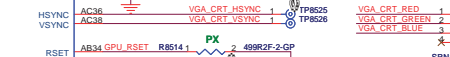
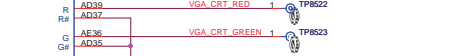
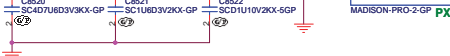
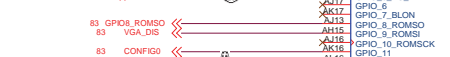
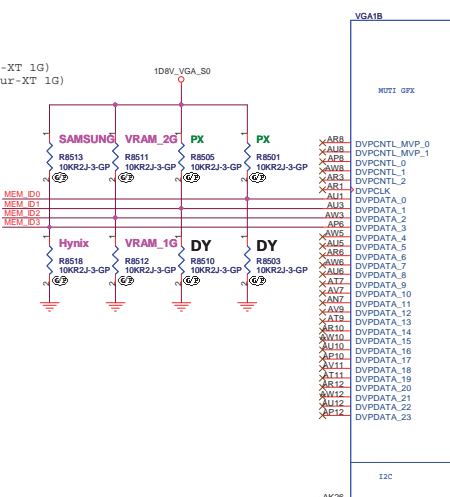
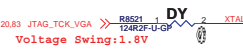
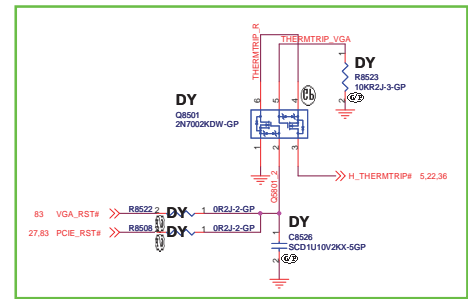
Sheet 82 of

4



DVPDATA [3:2:1:0] for VRAM type
selection B/W strap
Should provide VRAM Table for VBIOS request

DVPDATA [3:0]
0111 2Gbit Hynix-H5TQ2G63BFR-12C (800MHz) (Whistler-LP 2G / Seymour-XT 1G)
1111 2Gbit Samsung-K4W2G1646C-HC12 (800MHz) (Whistler-LP 2G / Seymour-XT 1G)
0011 1Gbit Hynix-H5TQ1G63BFR-12C (800MHz) (Whistler-LP 1G)
1011 1Gbit Samsung-K4W1G1646E-HC12 (800MHz) (Whistler-LP 1G)

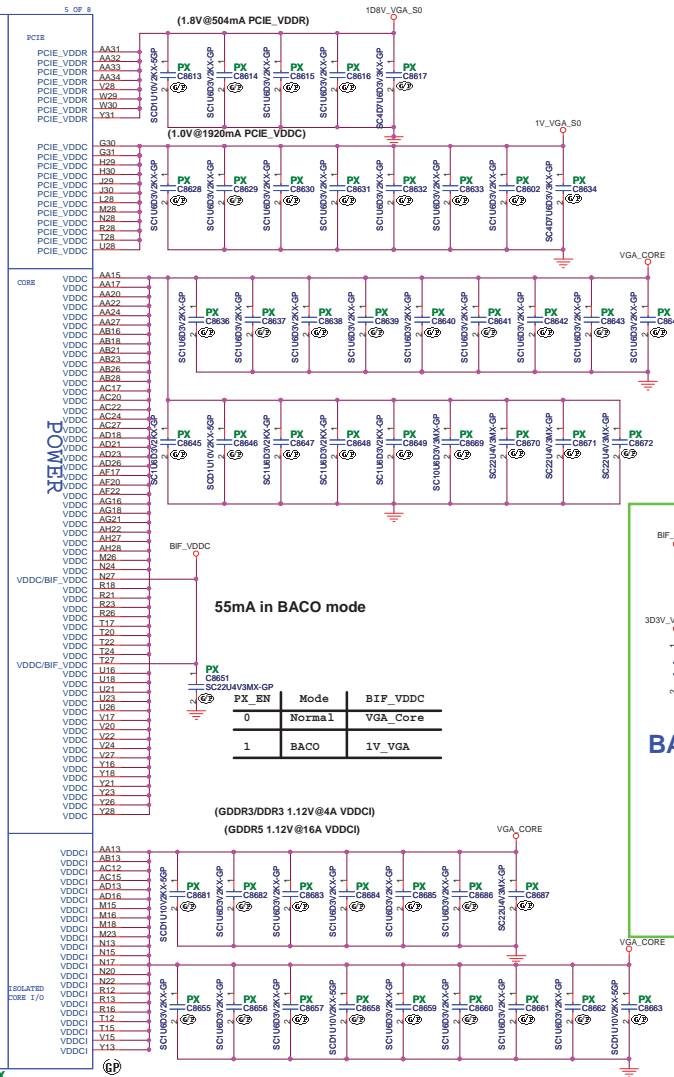
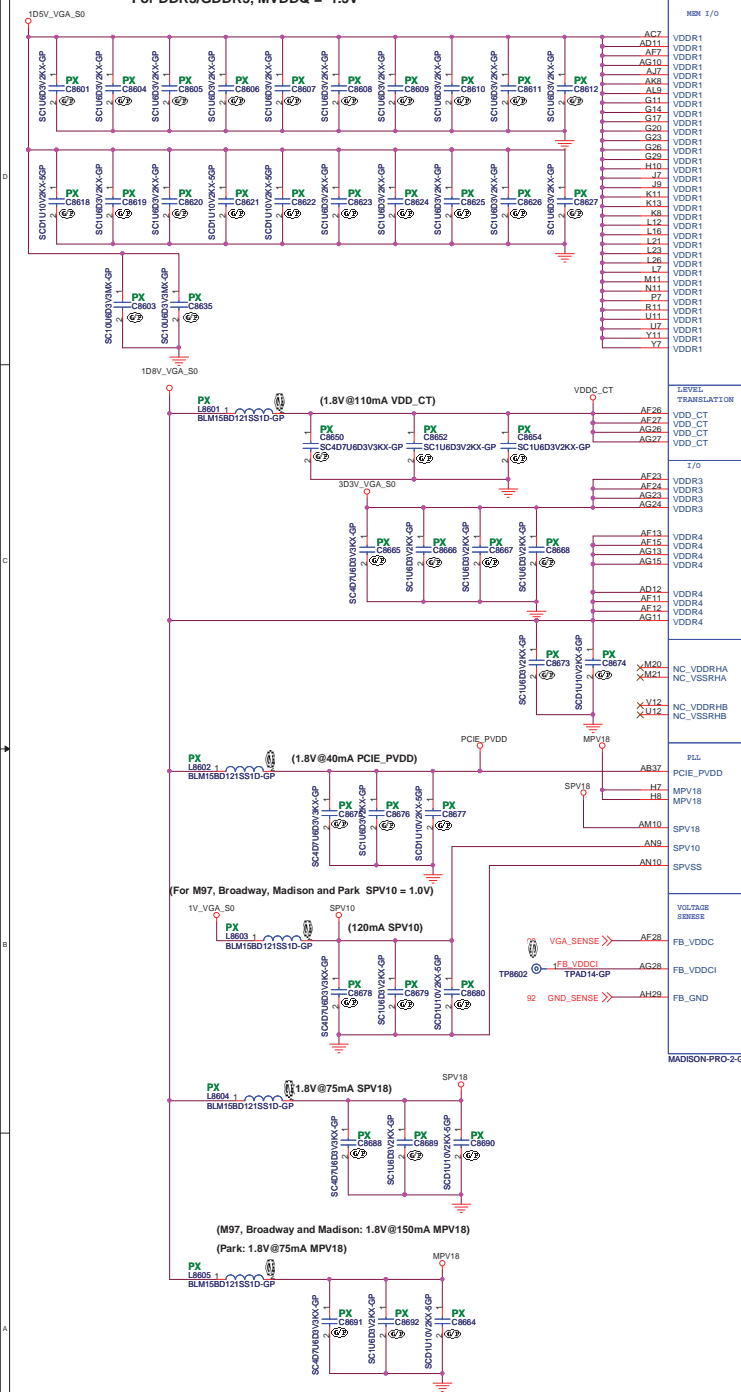


Clock Input Configariton -GDDR3/DDR3

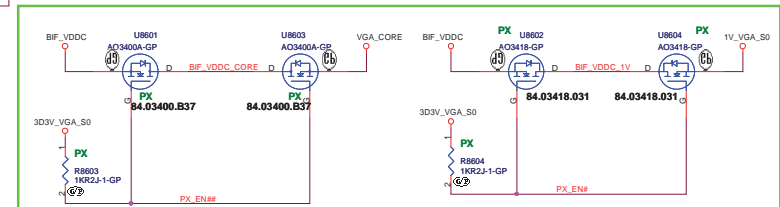
a) 27MHz crystal connected to XTALIN or XTALOUT or

b) 27MHz (1.8V) oscillator connected to XTALIN or

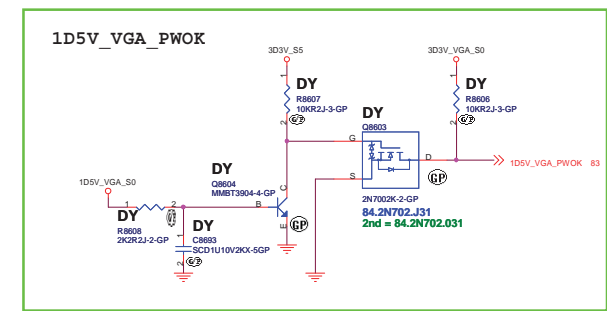
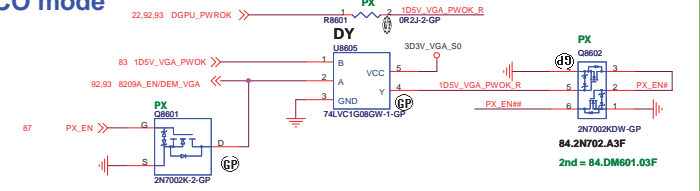
c) 27MHz (3.3V) oscillator connected to XO_IN (Park, Madison, and Broadway only)

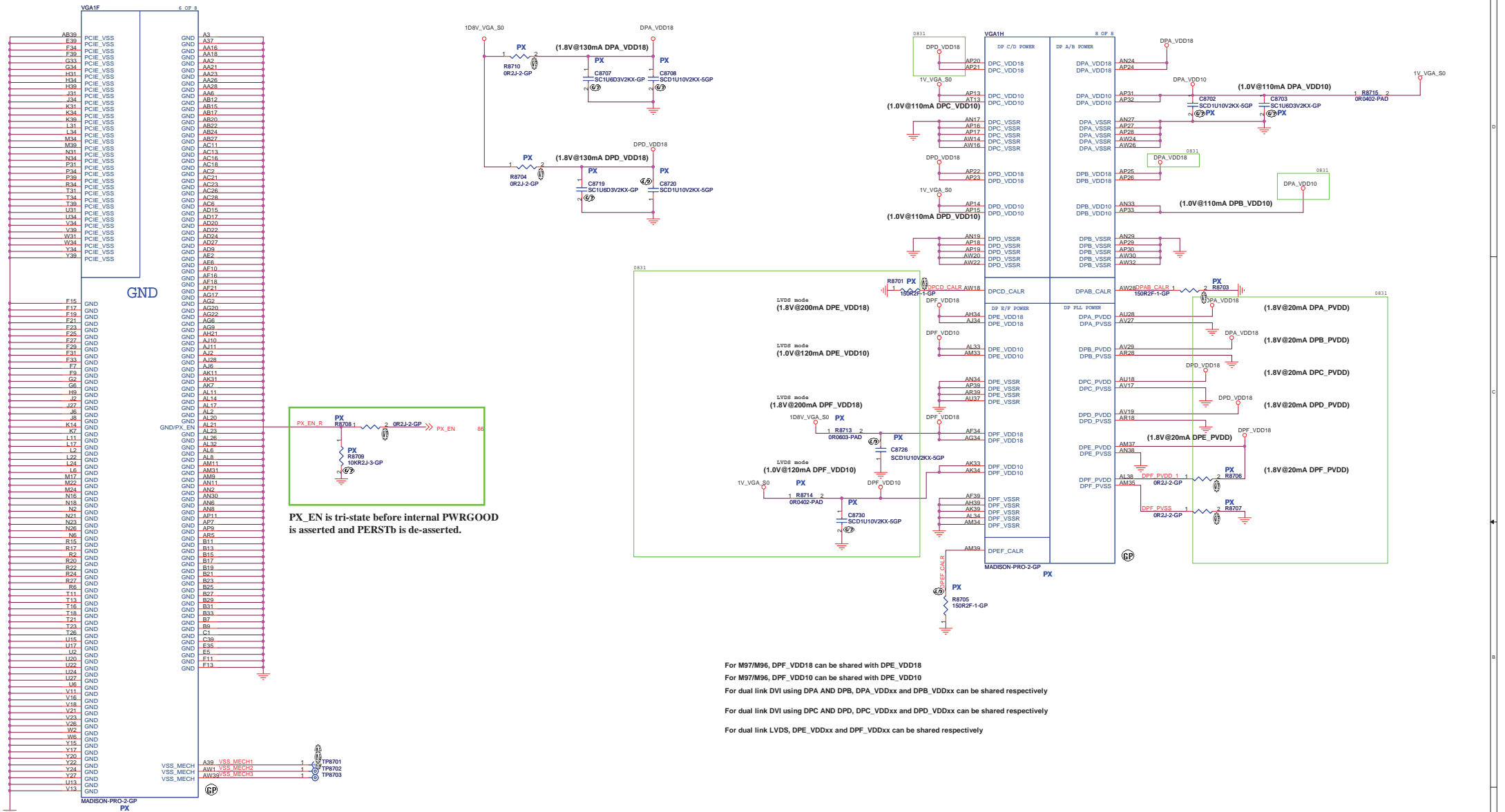


dGPU Power Pins	Voltage	In BACO Mode
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F-E]_VDDI8, DP[D-A]_PVDD, DP[D-A]_VDDI8, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	ON
DP[F-E]_VDDI0, DP[D-A]_VDDI0, DPLL_VDDC, and SPV10	1.0V	ON
PCIE_VDDC	1.0V	ON
VDDR3 and A2VDD	3.3V	ON
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	ON (Same as PCIE_VDDC)
VDDR1	1.8V/1.5V	OFF
VDDC/VDDCI	0.85-1.15V	OFF

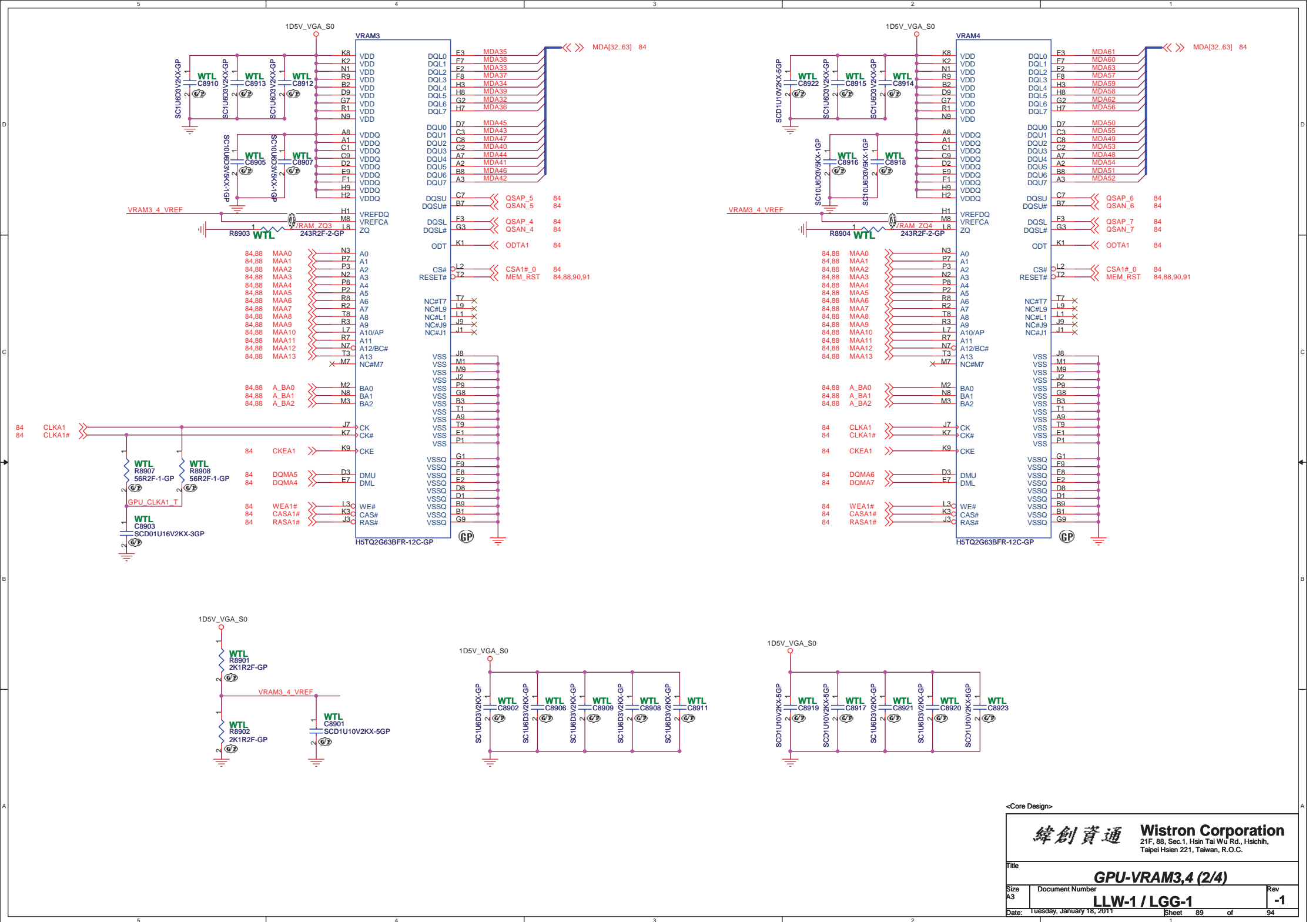


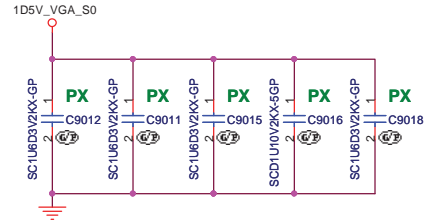
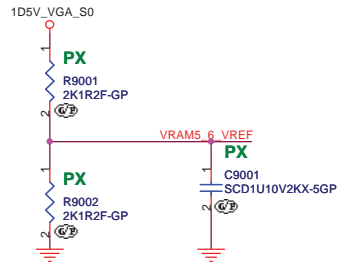
BACO mode

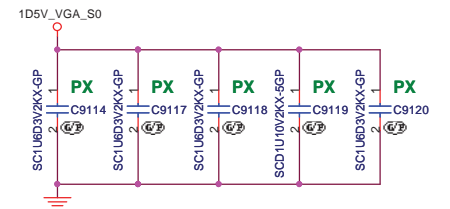
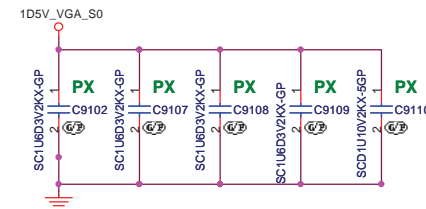
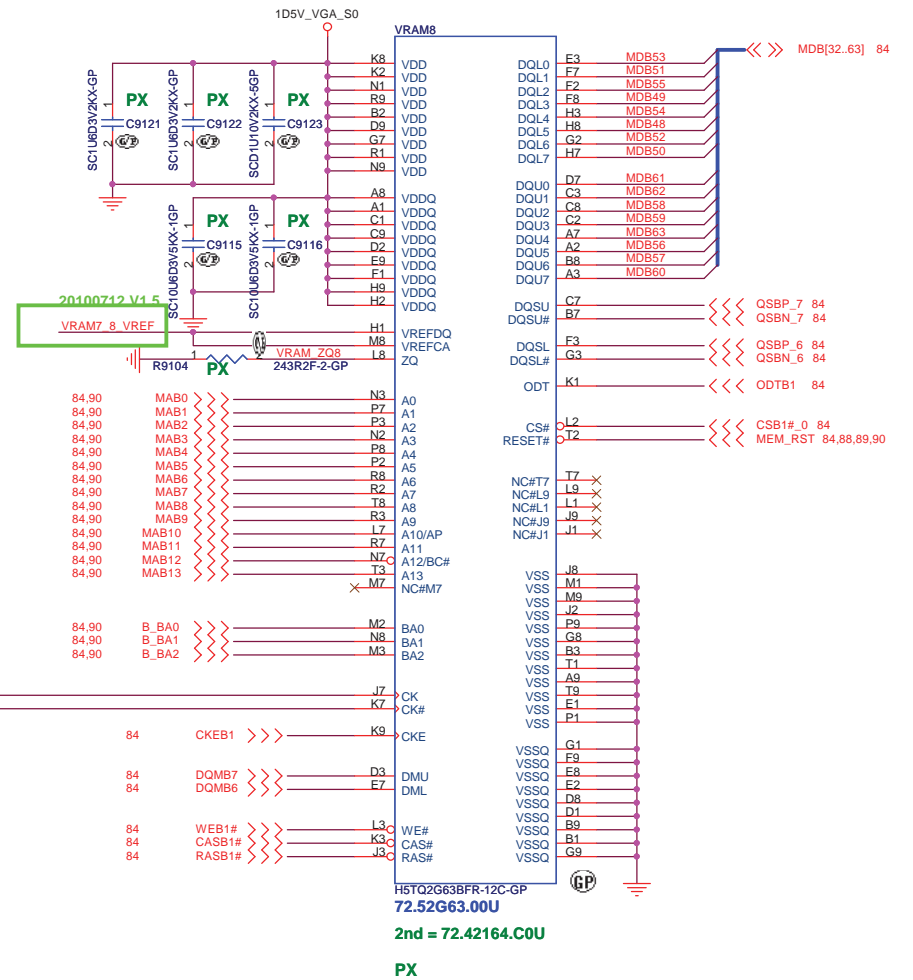
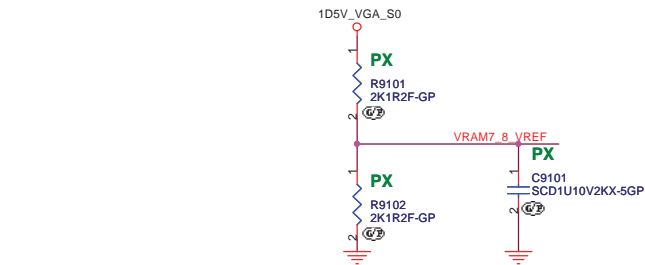
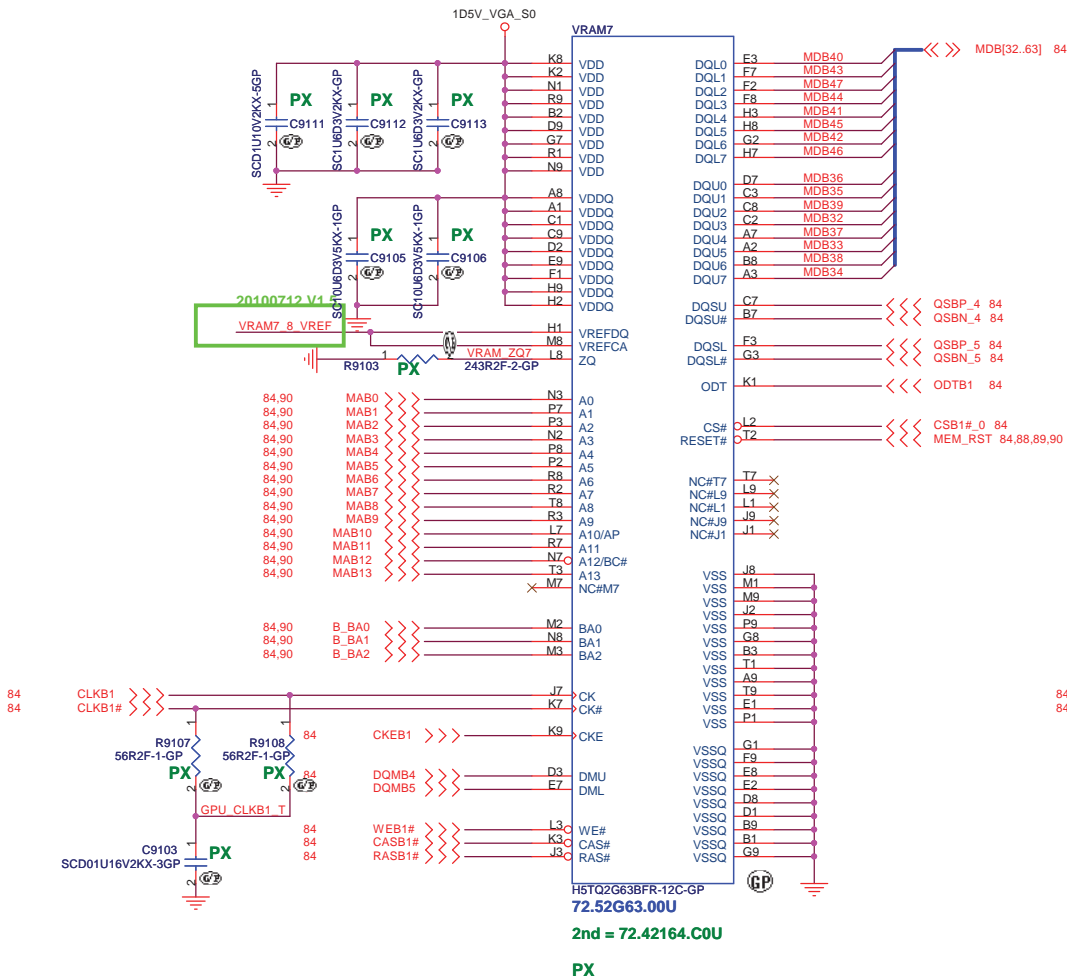




For M97/M96, DPF_VDD18 can be shared with DPE_VDD18
For M97/M96, DPF_VDD10 can be shared with DPE_VDD10
For dual link DVI using DPA AND DPB, DPA_VDDxx and DPB_VDDxx can be shared respectively
For dual link DVI using DPC AND DPD, DPC_VDDxx and DPD_VDDxx can be shared respectively
For dual link LVDS, DPE_VDDxx and DPF_VDDxx can be shared respectively





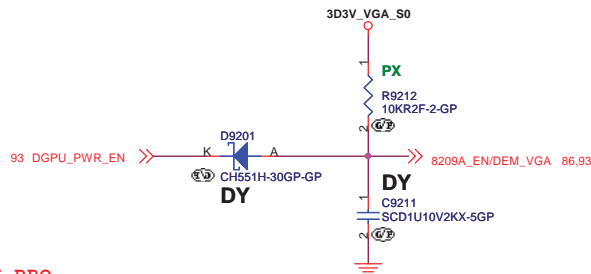
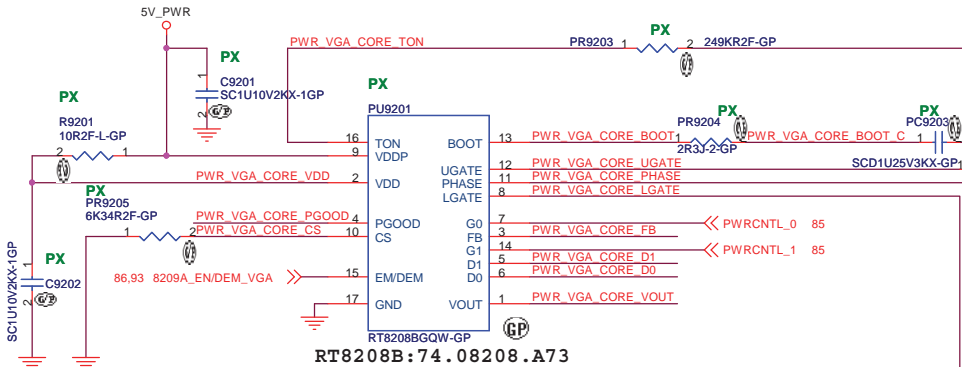
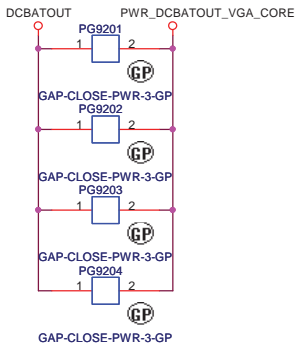


<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			GPU-VRAM7,8 (4/4)	
Size	Document Number	LLW-1 / LGG-1		Rev
A3				-1
Date:	1 Tuesday, January 18, 2011	Sheet	91	of 94

```
SSID = PWR.Plane.Regulator_GFX
```

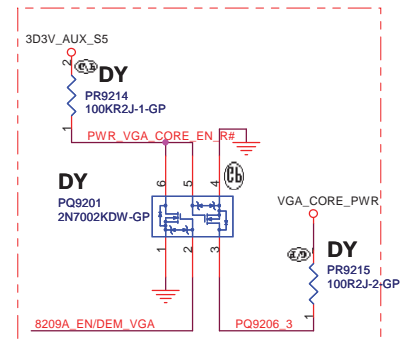
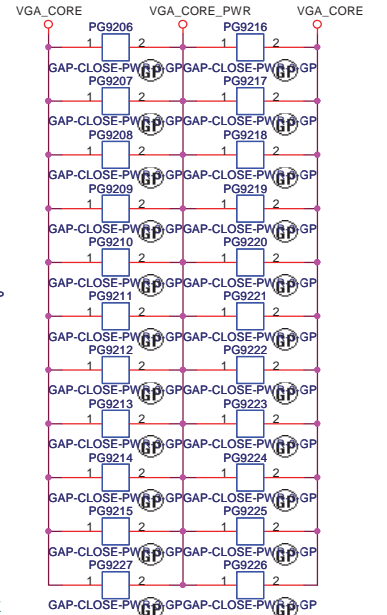
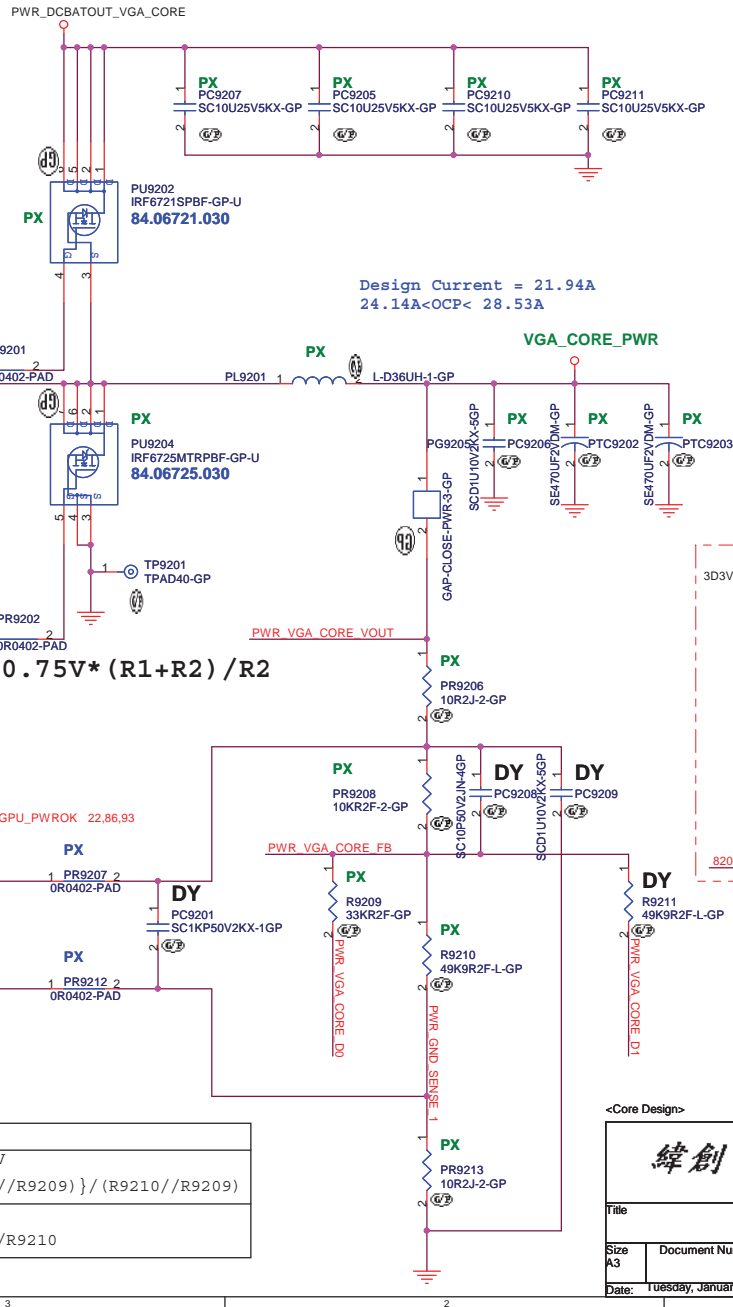


MADSION PRO

Setting Vref Vout & Rfb-Top	Vref (V)	R9208	R9210	R9211	R9209
	0.75	10K	50K	50K	75K
VOUT (Target)	VOUT (compute)			VID1	VID0
1.150	1.150			0	0
1.050	1.050			0	1
1.000	1.000			1	0
0.900	0.900			1	1

```
WHIST => R9211 NO_ASM.  
SEYMR => whole ASM
```

NVVDD_ALTV1	NVVDD_ALTV0	+VGA_CORE
H	L	1.12V or 1V OUT= $[R9208 + (R9210 // R9209)] / (R9210 // R9209)$
H	H	0.9V OUT= $(R9208 + R9210) / R9210$

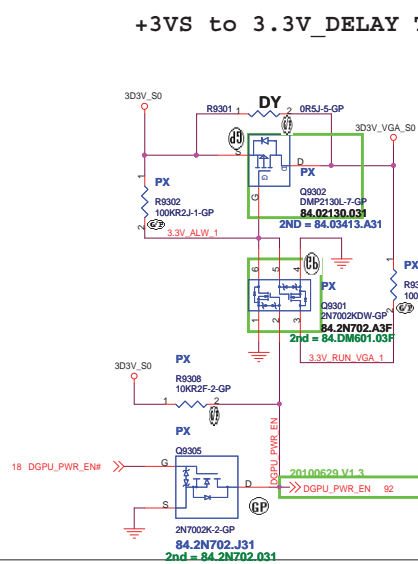


<Core Design>

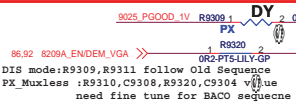
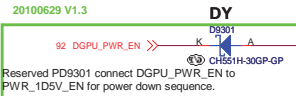
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
RT8208B +VGA CORE			
Size A3	Document Number		Rev
	LLW-1 / LGG-1		-1
Date:	Tuesday, January 18, 2011	Sheet 92 of 94	

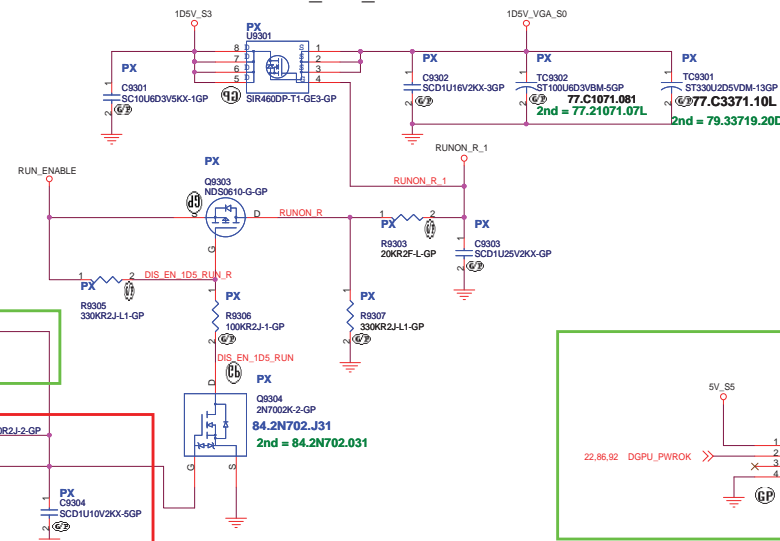
+3VS to 3.3V_DELAY Transfer



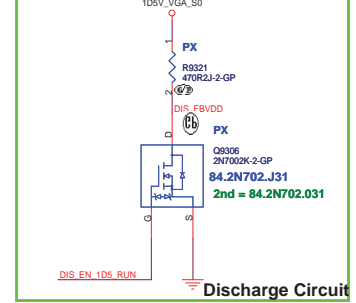
20100629 V1.3



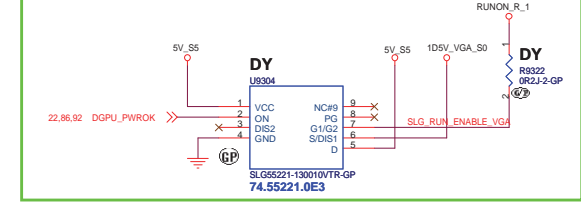
1D5V_VGA_S0



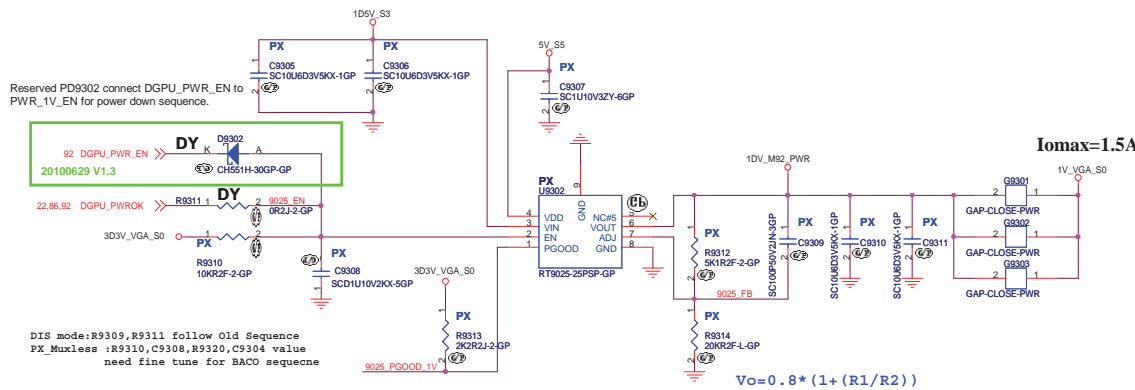
20100629 V1.3



20100805 V1.8



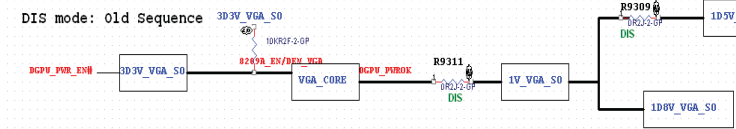
RT9025 for 1V_VGA



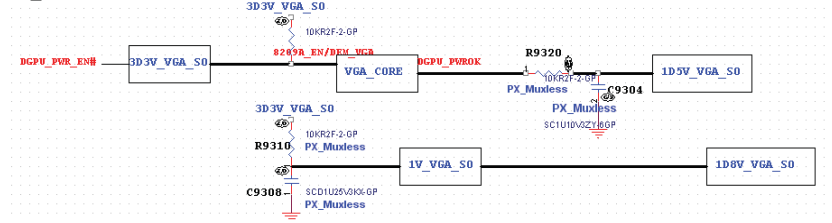
Iomax=1.5A

$$V_O = 0.8 * (1 + (R1/R2))$$

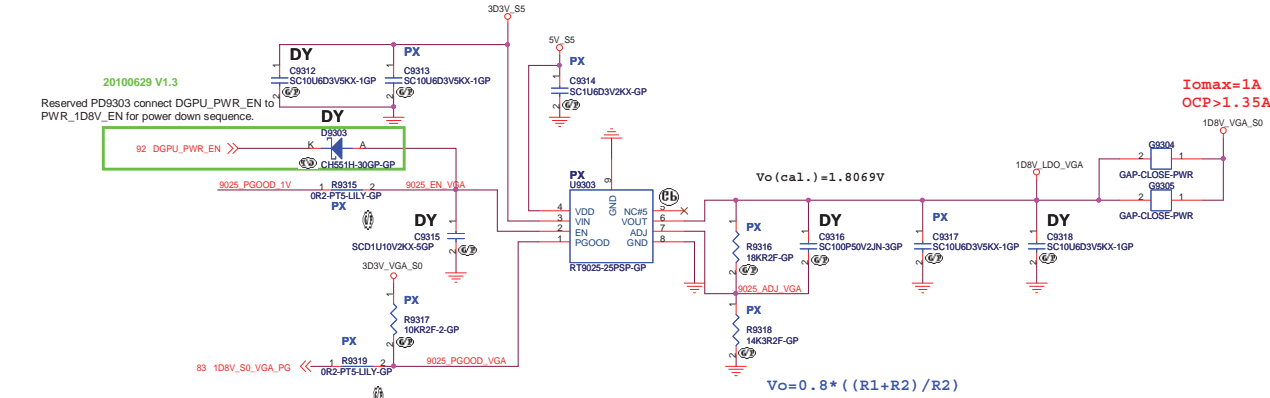
DIS mode: Old Sequence



PX_Muxless : value need fine tune for BACO sequece



RT9025 for 1D8V_VGA



Iomax=1A
OCP>1.35A

$$V_O(\text{cal.}) = 1.8069V$$

$$V_O = 0.8 * ((R1+R2) / R2)$$

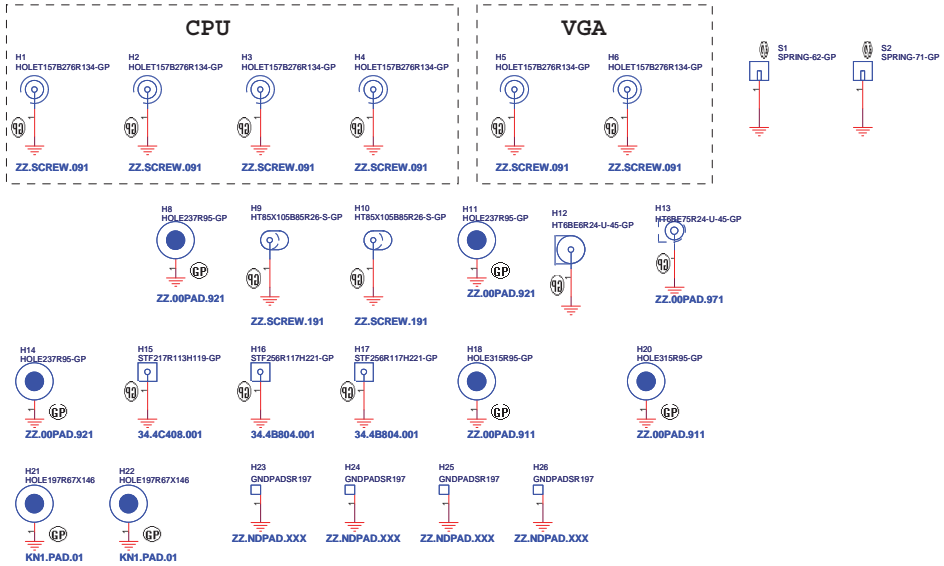
Table 93.1- Adjustable LDO Regulator multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
GMT	G9661-25ADJF11U	N/A	74.09661.07D
RICHTER	RT9025-25GSP	N/A	74.09025.A3D

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.

File	Document Number	Rev
	LLW-1 / LGG-1	-1
Date: Tuesday, January 18, 2011	Sheet 93 of 94	



EMI CAP

